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# LCFC Confidential

## GS454/GS554(NMD031) MB Schematics Document

### ICL U42 with DDR4 + Nvidia N16V-GM

2019-10

REV:0.1

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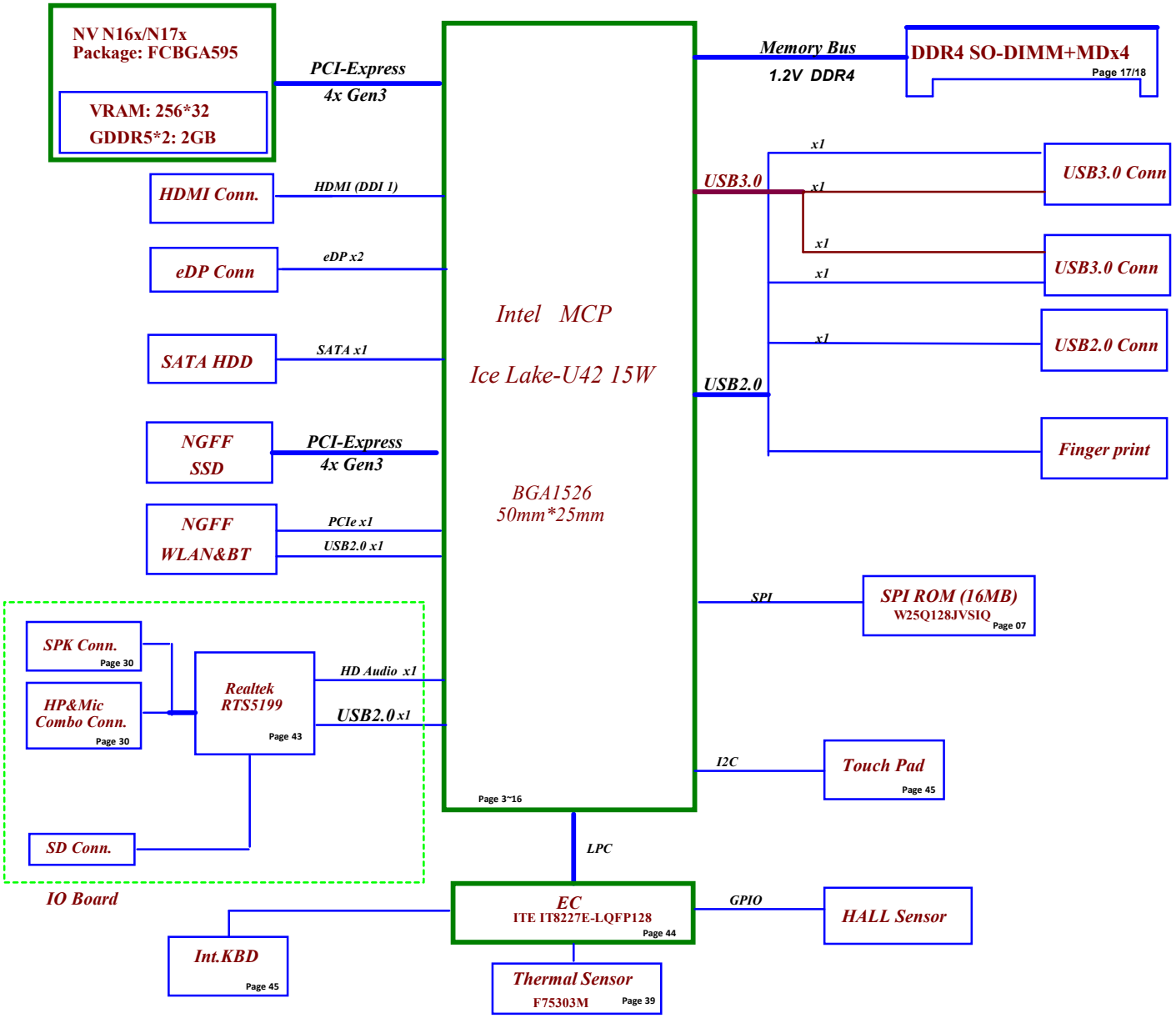


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Title: Block Diagram

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## Voltage Rails ( O --> Means ON , X --> Means OFF )

| Power Plane / State | V9B+ | +3VALW<br>+5VALW<br>+3VALW_PCH<br>+1.8VALW<br>VCC_AUX | +1.2V<br>+2.5V_DDR<br>+VCCST<br>+VCCSTG | +5VS<br>+3VS<br>+1.8VS<br>+CPU_CORE<br>+0.6VS |
|---|---|---|---|---|
| S0 | O | O | O | O |
| S3 | O | O | O | X |
| S3 Battery only | O | O | O | X |
| S5 S4 AC Only | O | O | X | X |
| S5 S4 Battery only | O | X | X | X |
| S5 S4 AC & Battery don't exist | X | X | X | X |

| STATE \ SIGNAL | | SLP_S3# | SLP_S4# | SLP_S5# | +VALW | +V | +VS | Clock |
|---|---|---|---|---|---|---|---|---|
| Full ON | | HIGH | HIGH | HIGH | ON | ON | ON | ON |
| S3 (Suspend to RAM) | | LOW | HIGH | HIGH | ON | ON | OFF | OFF |
| S4 (Suspend to Disk) | | LOW | LOW | LOW | ON | OFF | OFF | OFF |
| S5 (Soft OFF) | | LOW | LOW | LOW | ON | OFF | OFF | OFF |
| | | | | | | | | |

| HSIO PORT | | Function |
|---|---|---|
| USB3.0 | 1 | USB3.0 Conn |
| | 2 | USB3.0 Conn |
| | 3 | NC |
| | 4 | NC |
| | 5 | |
| | 6 | |
| USB2.0 | 1 | USB3.0 Conn |
| | 2 | USB3.0 Conn |
| | 3 | NC |
| | 4 | NC |
| | 5 | Camere |
| | 6 | Touch Screen |
| | 7 | Finger Print |
| | 8 | Card Reader |
| | 9 | USB2.0 conn |
| | 10 | Bluetooth |
| PCIE | 5~8 X4 | DGPU |
| | 9 | WLAN |
| | 10 | NC |
| | 11 | SATA HDD |
| | 12 | NC |
| | 13~16 X4 | PCIE/SATA SSD |

| BOM Structure | BTO Item |
|---|---|
| @ | Un-stuff |
| 14@ | For 14" part |
| 15@ | For 15" part |
| CD@ | For cost down |
| EMC@ | For EMC part |
| EMC_15@ | For EMC 15" part |
| EMC_NS@ | For EMC un-stuff part |
| ME@ | For ME part |
| UMA@ | For UMA part |
| OPT@ | For NV GPU part |
| OPTN16@ | For NV N16S-GTR GPU part |
| OPTN17@ | For NV N17S-G1 GPU part |
| TS@ | For touch screen part |
| TP@ | For TOuch Pad Part |

## SMBUS Control Table

| | SOURCE | BATT | Charger | DGPU | IT8227E | Memory Down | PCH | PMIC | SODIMM | Thermal Sensor | WLAN WiMAX |
|---|---|---|---|---|---|---|---|---|---|---|---|
| EC_SMB_CK1<br>EC_SMB_DA1 | IT8227E<br>+3VL_EC | V | V | X | V<br>+3VL_EC | X | X | X | X | X | X |
| EC_SMB_CK0<br>EC_SMB_DA0 | IT8227E<br>+3VS | X | X | V<br>+3VG_AON | V<br>+3VS | X | X | X | X | V | X |
| EC_SMB_CK3<br>EC_SMB_DA3 | IT8227E<br>+3VAWL | X | X | X | V | X | X | V | X | X | X |
| PCH_SMB_CLK<br>PCH_SMB_DATA | PCH<br>+3VALW_PCH | X | X | X | X | X | V<br>+3VALW_PCH | X | V<br>+3VS | X | X |

### EC SMBus1 address

| Device | Address |
|---|---|
| Smart Battery | need to update |
| Charger | 0001 0010 b |

### EC SMBus2 address

| Device | Address |
|---|---|
| Thermal Sensor(NCT7718W) | 1001_100xb |
| DGPU | need to update |

### EC SMBus3 address

| Device | Address |
|---|---|
| PMIC | need to update |

### PCH SM Bus address

| Device | Address |
|---|---|
| DDR4 SODIMM | need to update |

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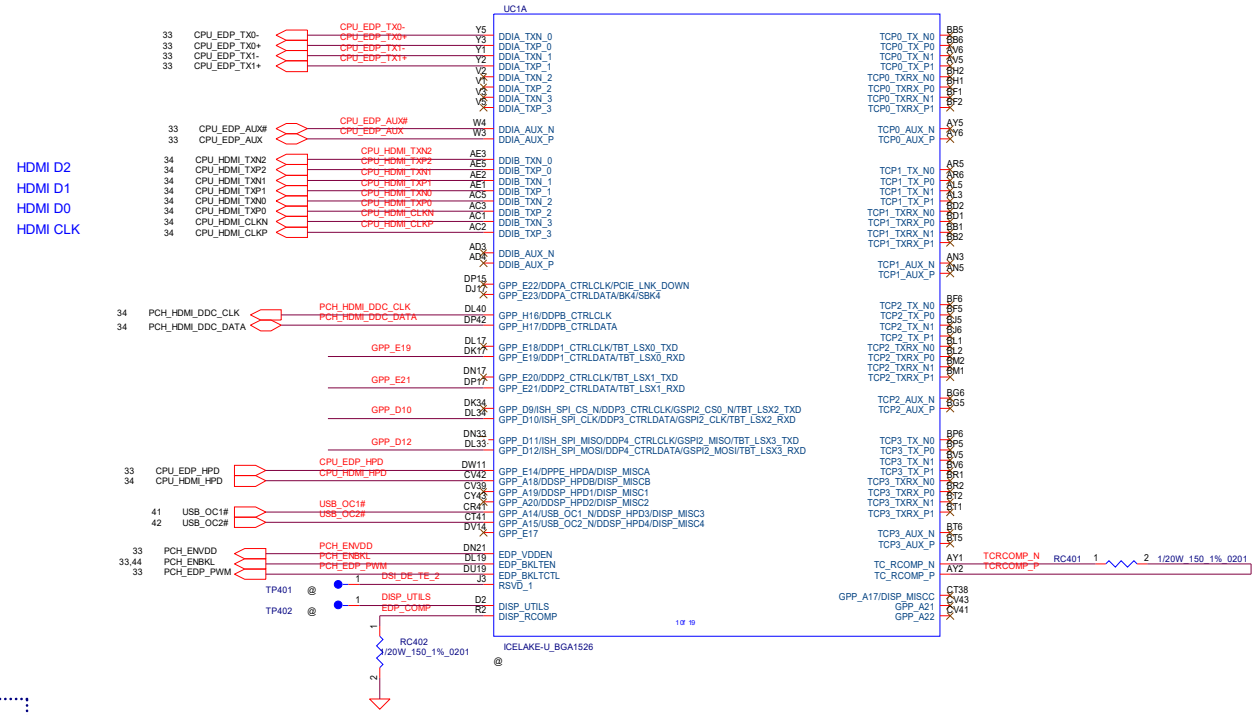

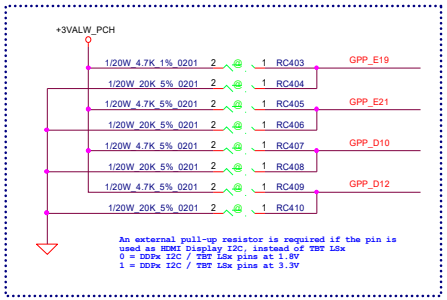


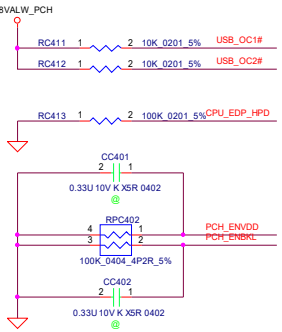


| GPIO Group | Power Supply |
|---|---|
| GPP_A | 1.8V |
| GPP_B/C/D/E | 3.3V |
| GPP_F | 1.8V(only) |
| GPP_G/H | 3.3V |
| GPP_R/S | 1.8V |
| GPD | 3.3V(only) |

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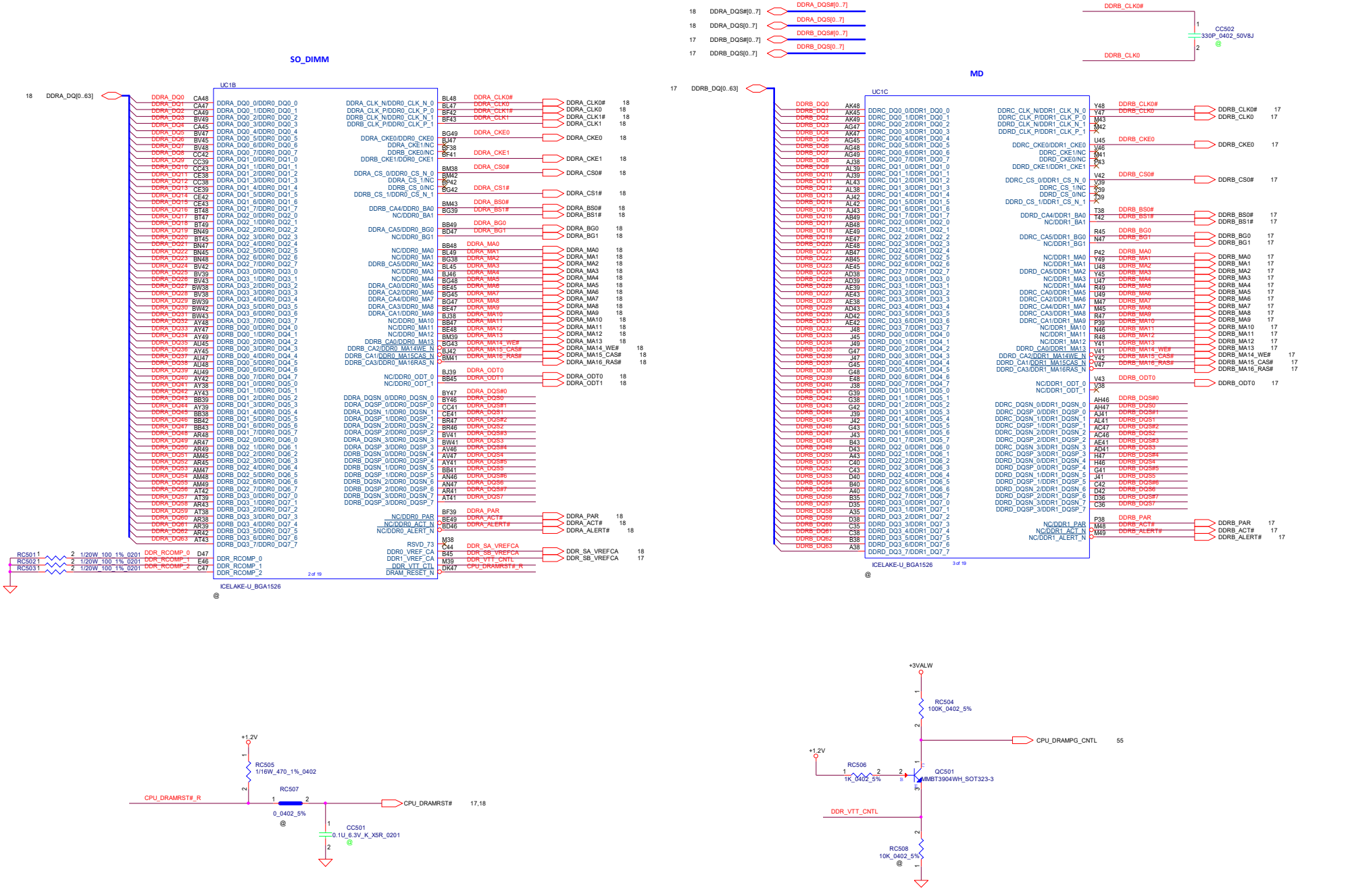


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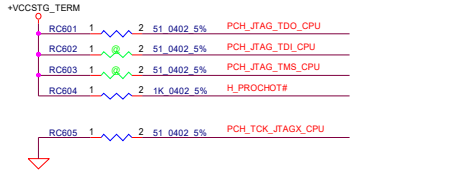


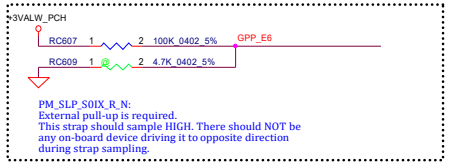


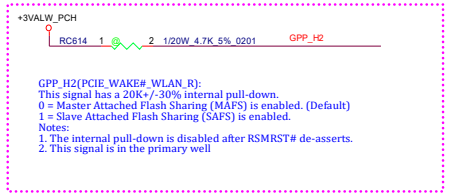

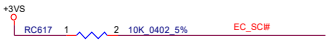


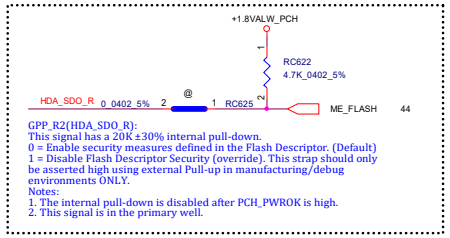


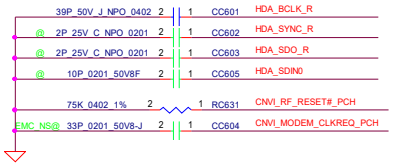


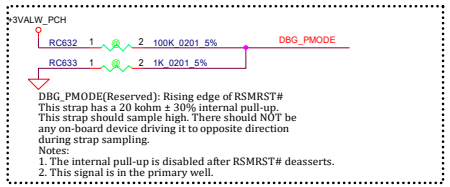


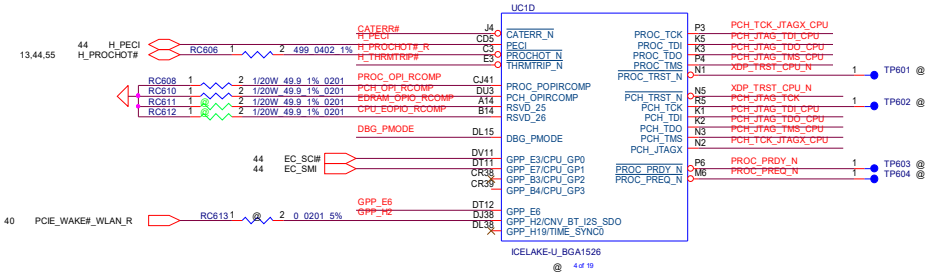


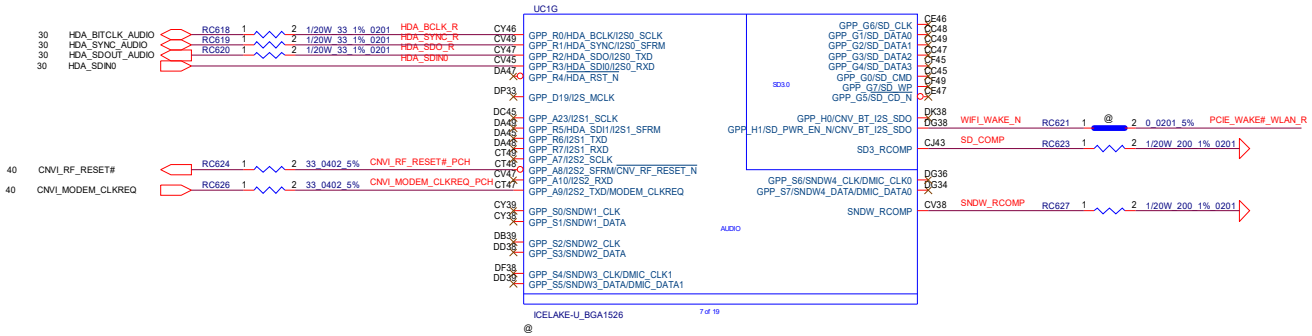


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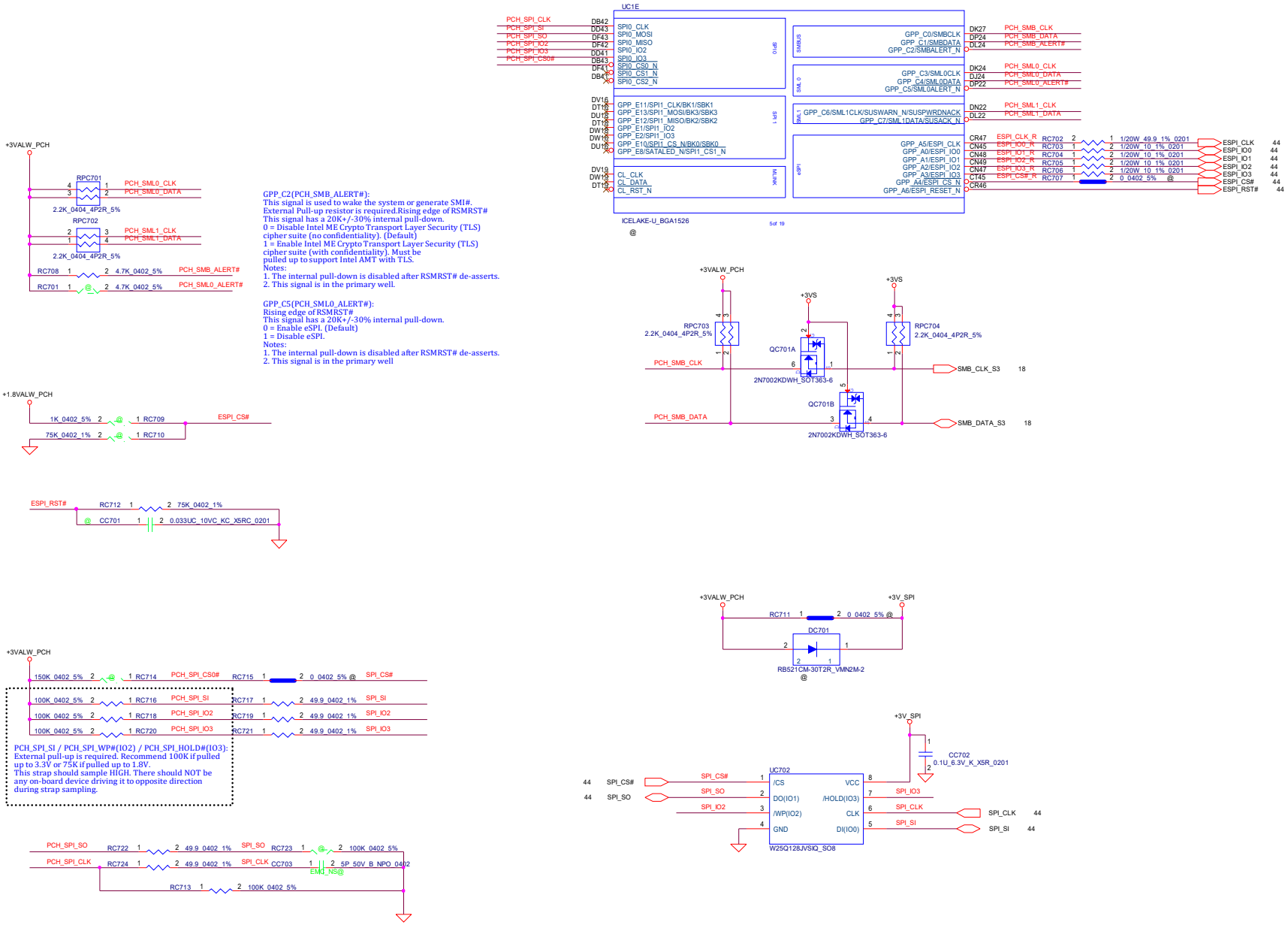


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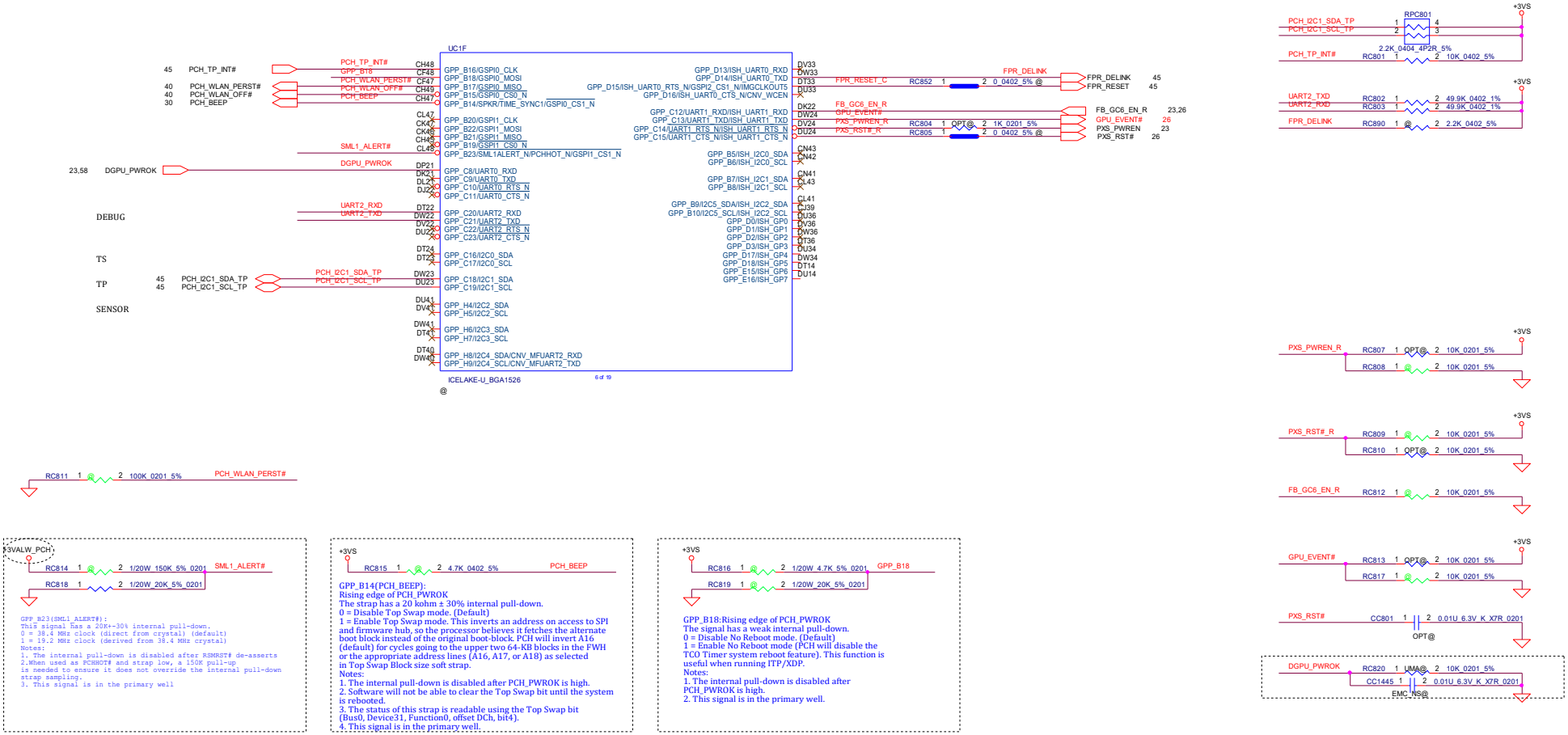


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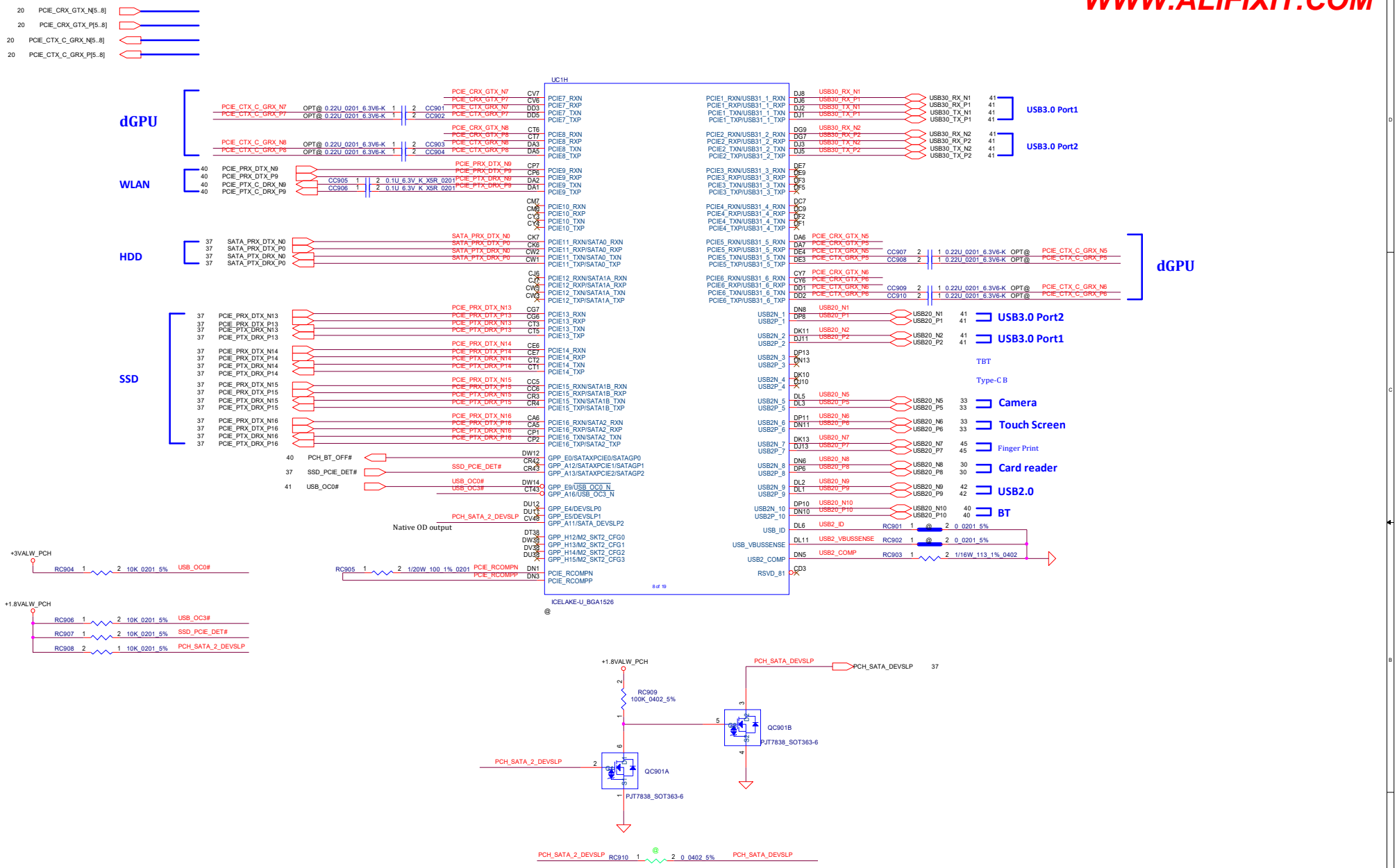


1. DEVSLP is an open-drain pin on the PCH side and is not required external pull-up orpull-down. The PCH will tri-state this pin to signal to the SATA device that it may enter a lower power state (pin will go high due to pull-up that's internal to the SATAdevice, per DEVSLP specification). PCH will drive pin low to signal an exit fromDEVSLP state.
2. DEVSLP is supported in direct connect, mSATA/mPCIe, uSSD, M.2.
3. 1 DEVSLP pin is required to support EACH DEVSLP enabled RAID storage device.
(Example: 2 DEVSLP pins are required to support 2 DEVSLP RAID storage devices).

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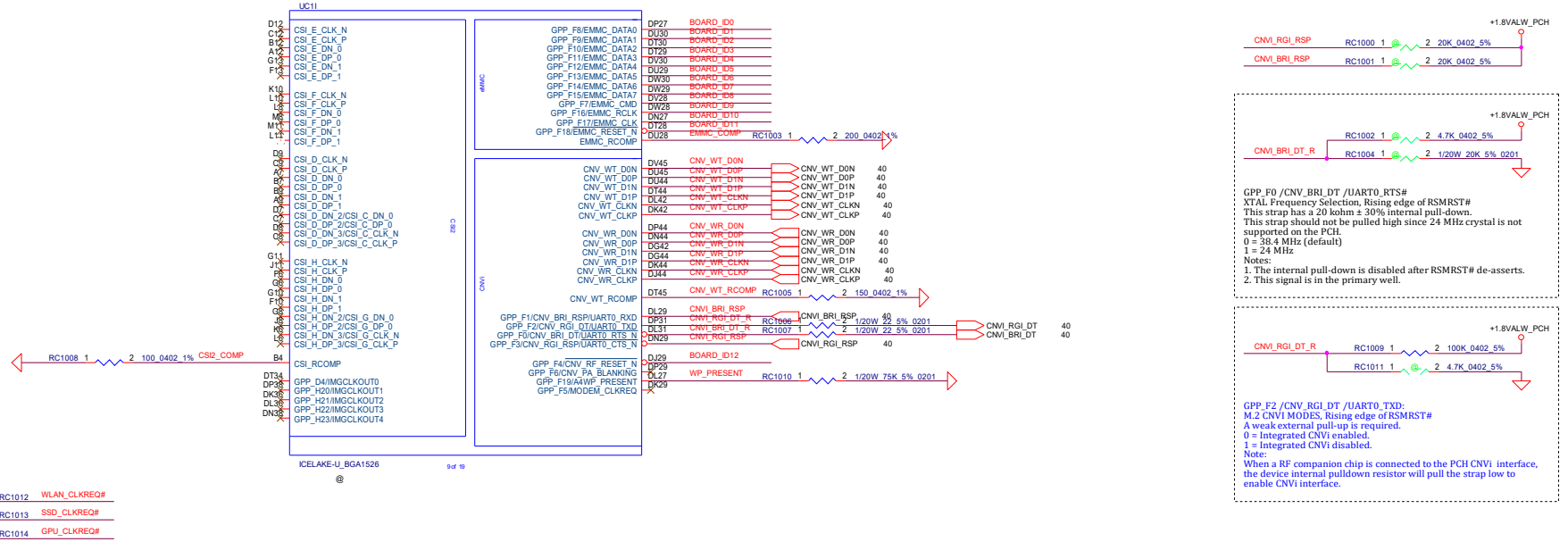


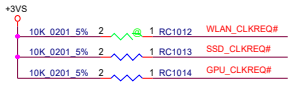


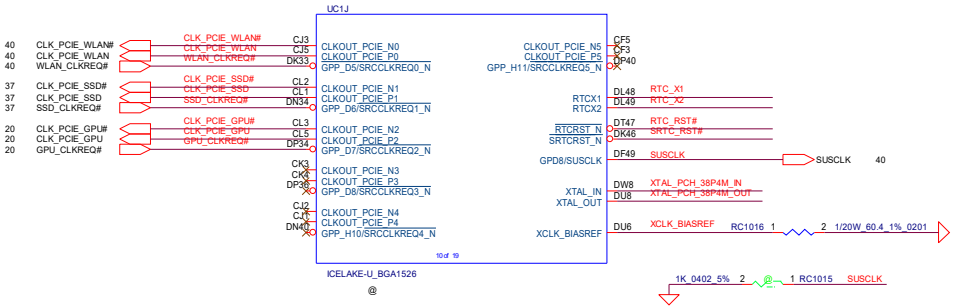


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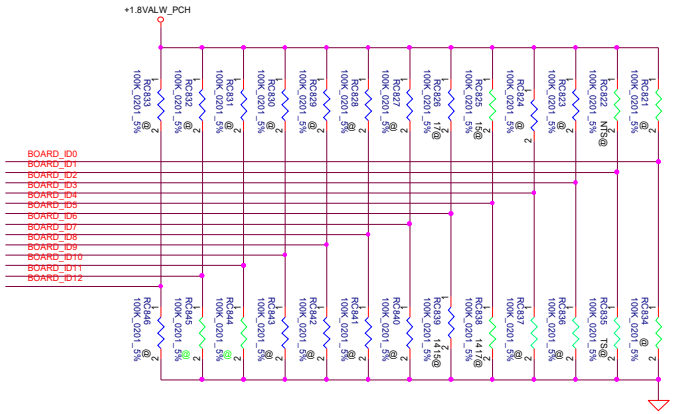
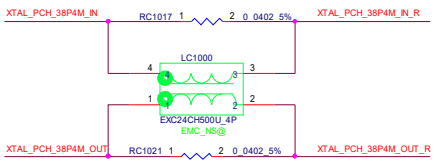
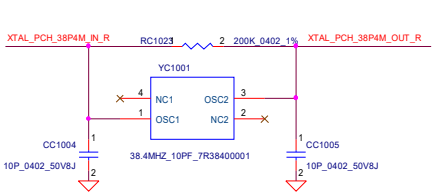
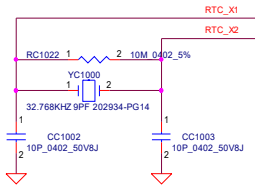
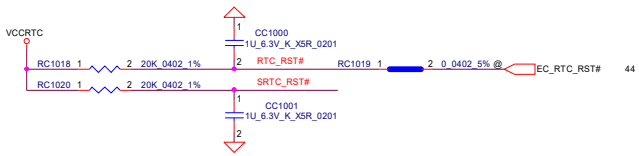



| | | |
|---|---|---|
| BOARD_ID5.4 | 14" | 00(R839,R838) |
| | 15" | 01(R839,R825) |
| | 17" | 10(R826,R838) |
| BOARD_ID6/7/8/9 | Sumsang | 0000 |
| | Hynix | 0001 |
| | Micron | 0010 |

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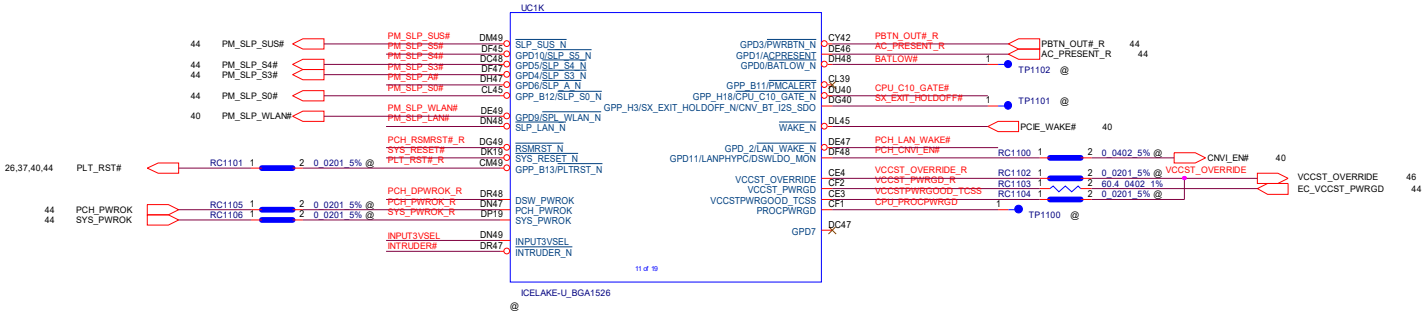
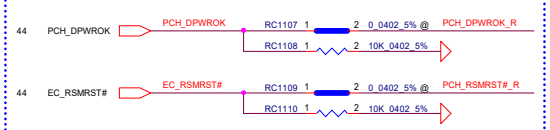
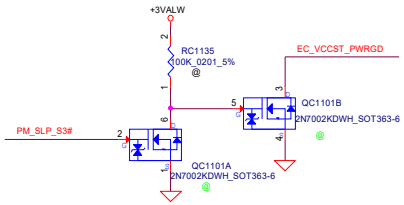
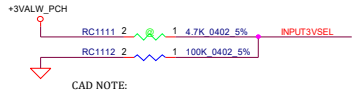


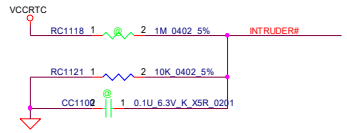

DSW_PWROK and RSMRST# are always separate power good signals



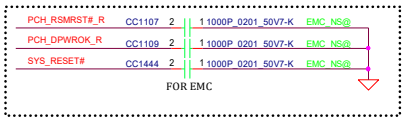




CAD NOTE:
INPUT3VSEL: 3V SELECT STRAP
LOW-> 3.3V +/-5%
HIGH->3.0V +/-5%




SPI Voltage Configuration:
The VCCSPI voltage (3.3V or 1.8V) is selected via a hard strap on the INTRUDER#.
This strap sets the SPI interface signaling voltage at the rising edge of RTCRST#. Designers should strap this pin to match the expected interface operational voltage for their target SPI device as follows.
0 = SPI interface operation voltage is 3.3V
(ground through a 10kohm resistor)
1 = SPI interface operation voltage is 1.8V
(pulled up with 1 Mohm to VCCRTC)



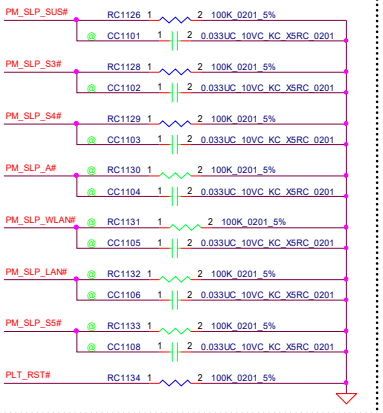

FOR EMC

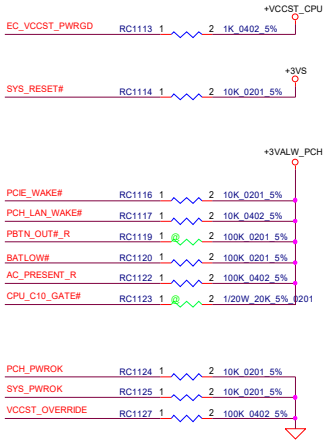
Glitch Free Requirements:
Pull-up resistor is required if a device is monitoring SLP_S0# before RSMRST# de-assertion
100K for 3.3V Signaling Mode
75K for 1.8V Signaling Mode

Glitch Free Requirements:
Cap or pull-down resistor is required

Option 1:Cap Implementation
330 nF for 3.3v Ramp Rate from 5-50ms
33 nF for 3.3V Ramp Rate Less than 5ms

Option 2:Pull-down Resistor Implementation
100K for 3.3V Signaling Mode
75K for 1.8V Signaling Mode

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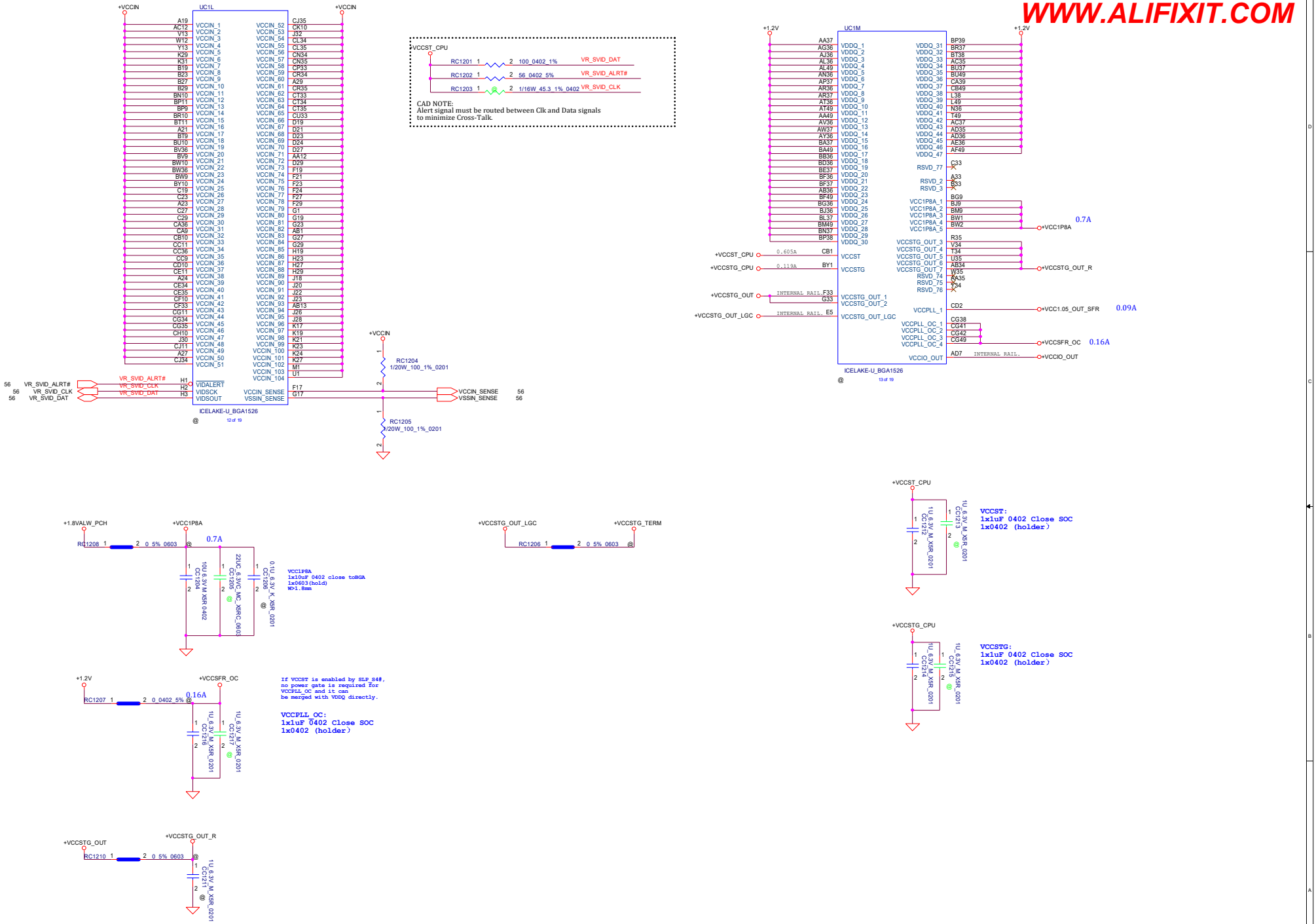


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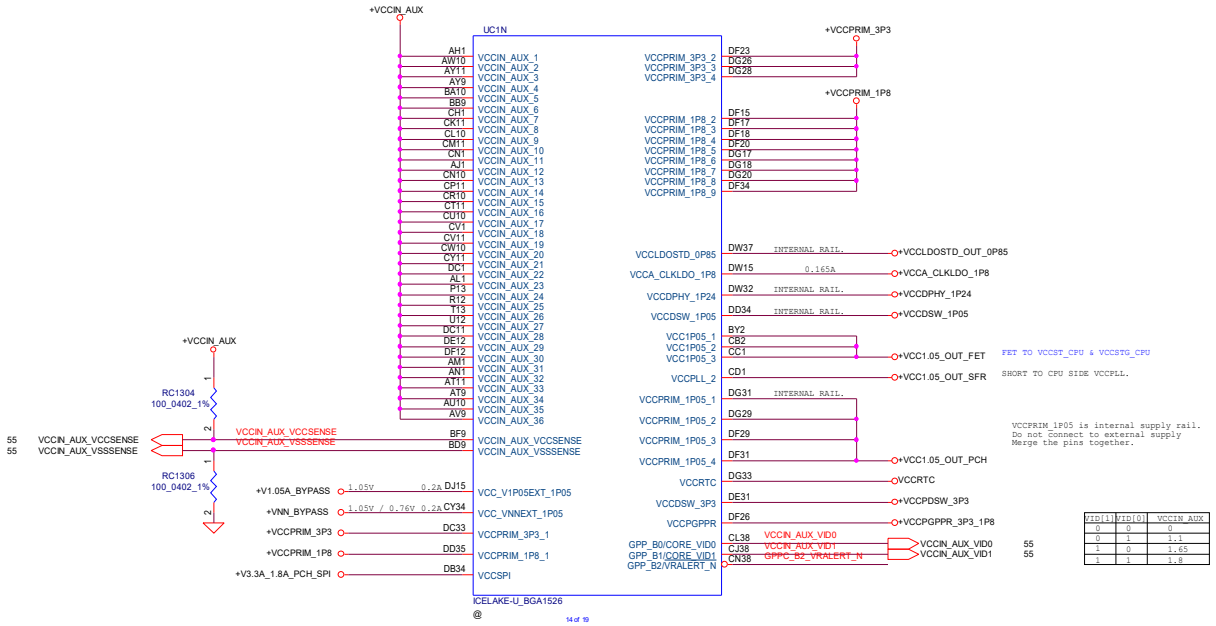
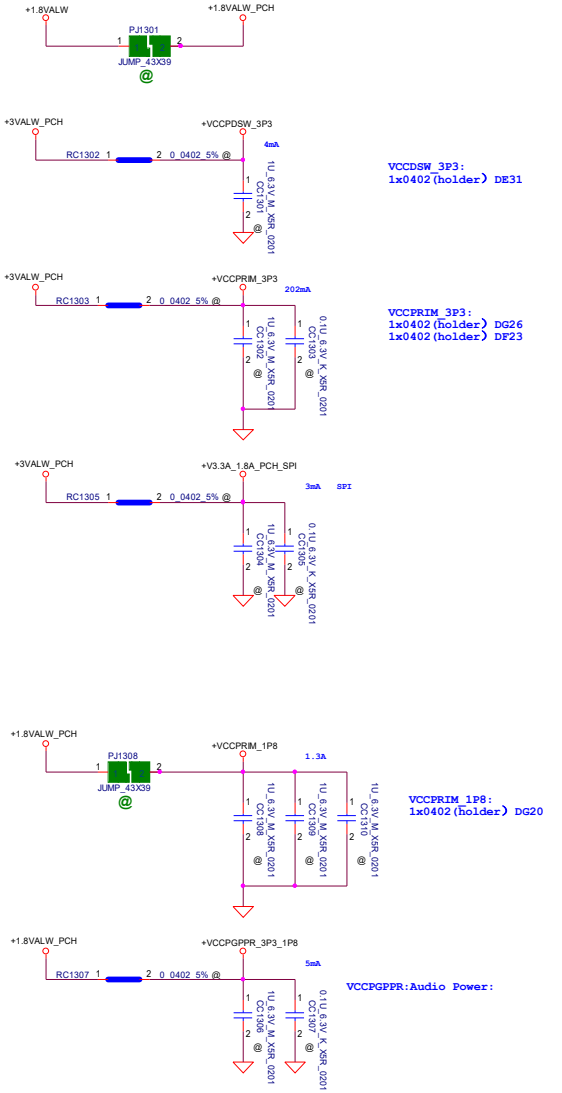
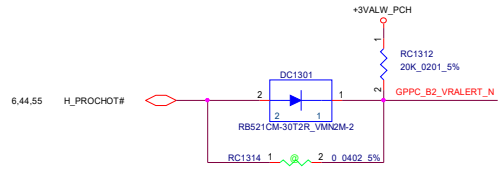
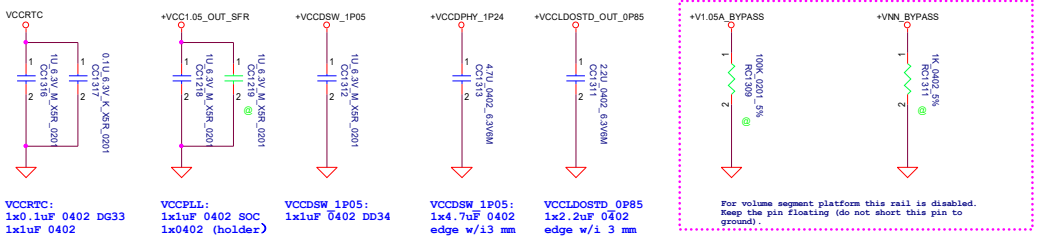
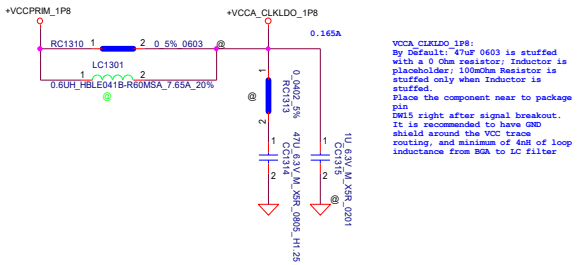



| VID[1] | VID[0] | VCCIN_AUX |
|---|---|---|
| 0 | 0 | 0 |
| 0 | 1 | 1.1 |
| 1 | 0 | 1.65 |
| 1 | 1 | 1.8 |

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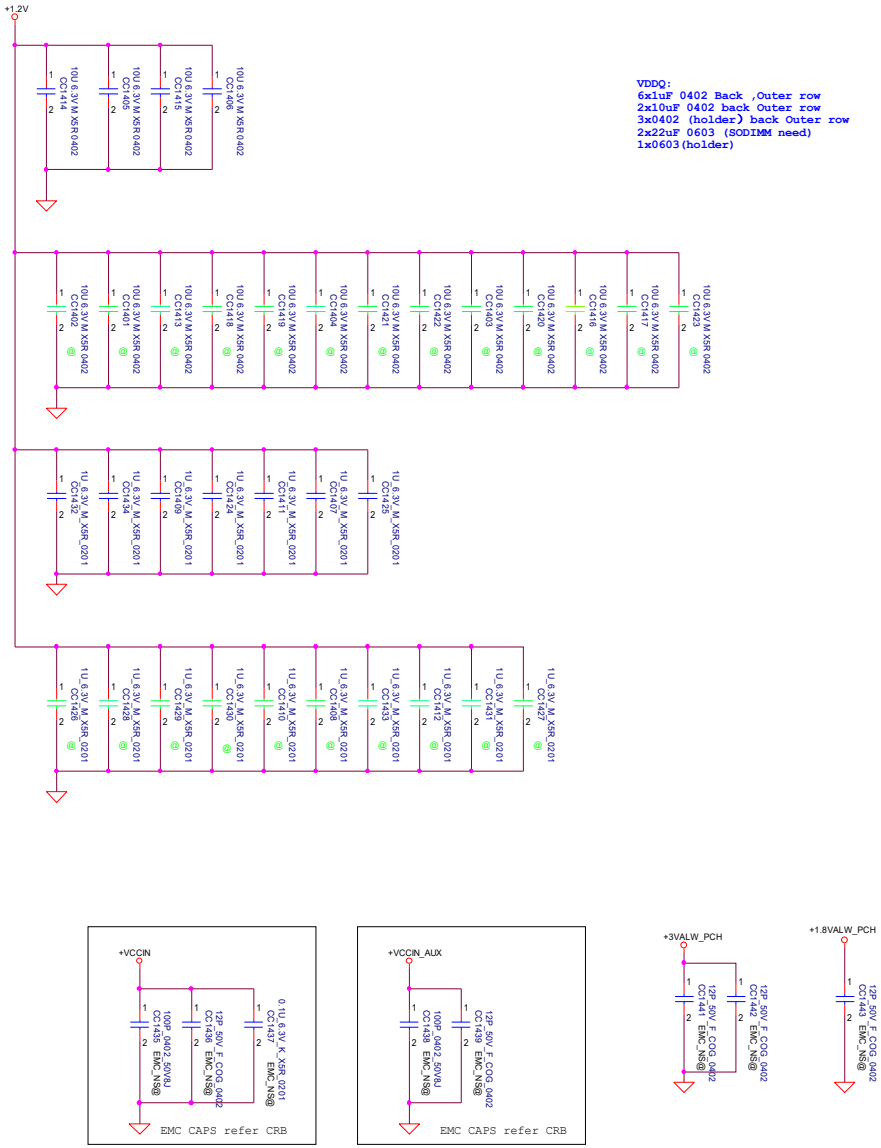


VDDQ:
6x1uF 0402 Back ,Outer row
2x10uF 0402 back Outer row
3x0402 (holder) back Outer row
2x22uF 0603 (SODIMM need)
1x0603(holder)

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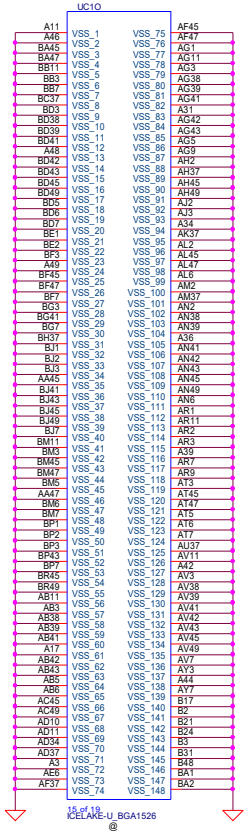


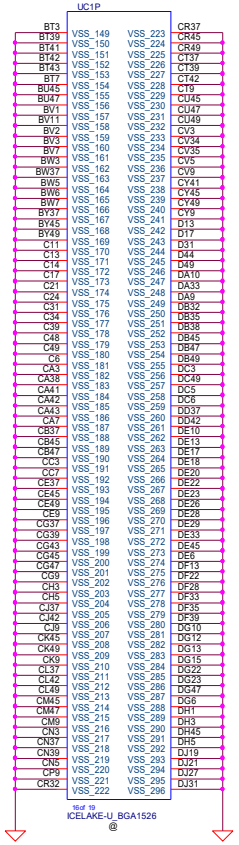


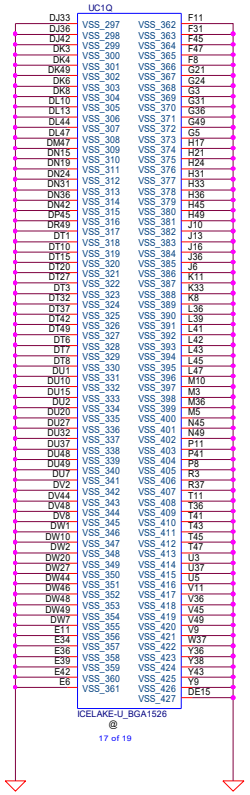


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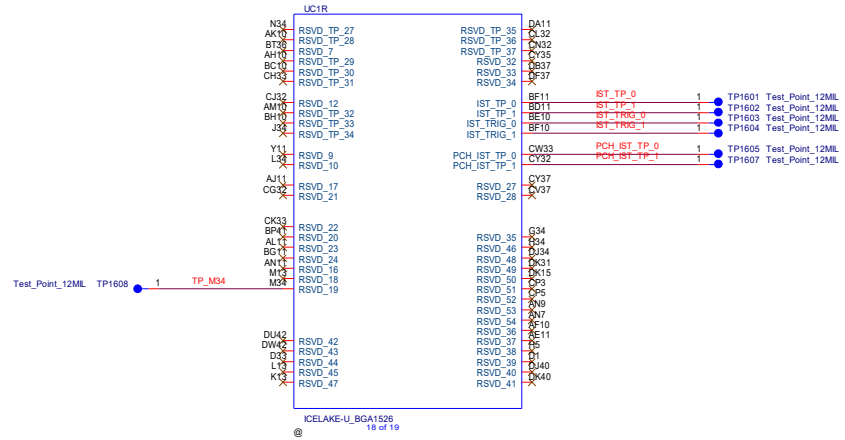
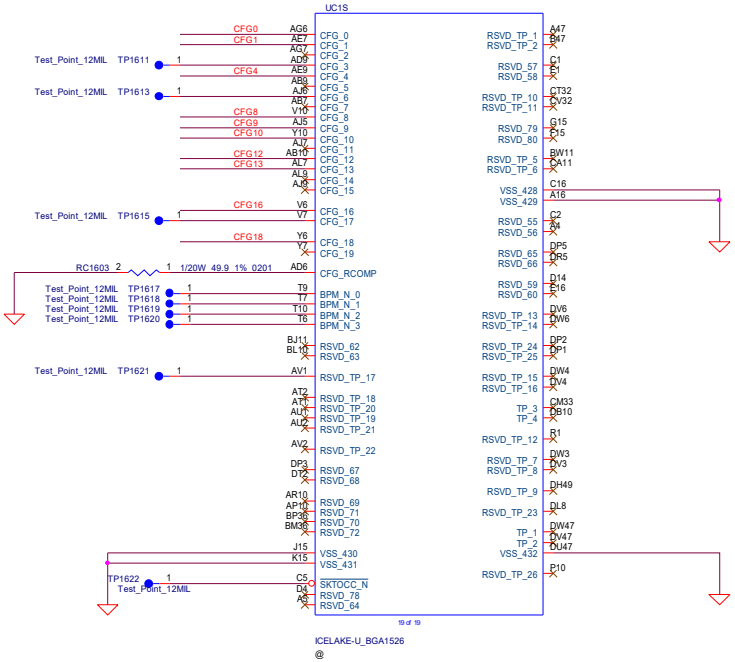
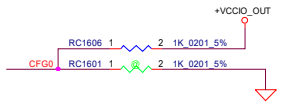
# PROCESSOR CFG STRAPS

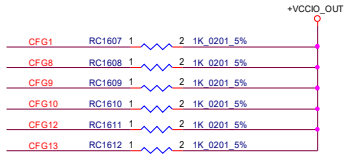


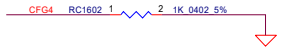




**Stall reset sequence after PCU PLL lock until de-asserted**

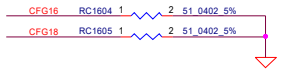
| | |
|---|---|
| CFG0 | 1:Normal(Default) * |
| | 0:Stall |




**Embedded Display Port Presence Strap**

| | |
|---|---|
| CFG4 | 1:Disable |
| | 0:Enable(Default) * |

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# DDR4 Memory Down

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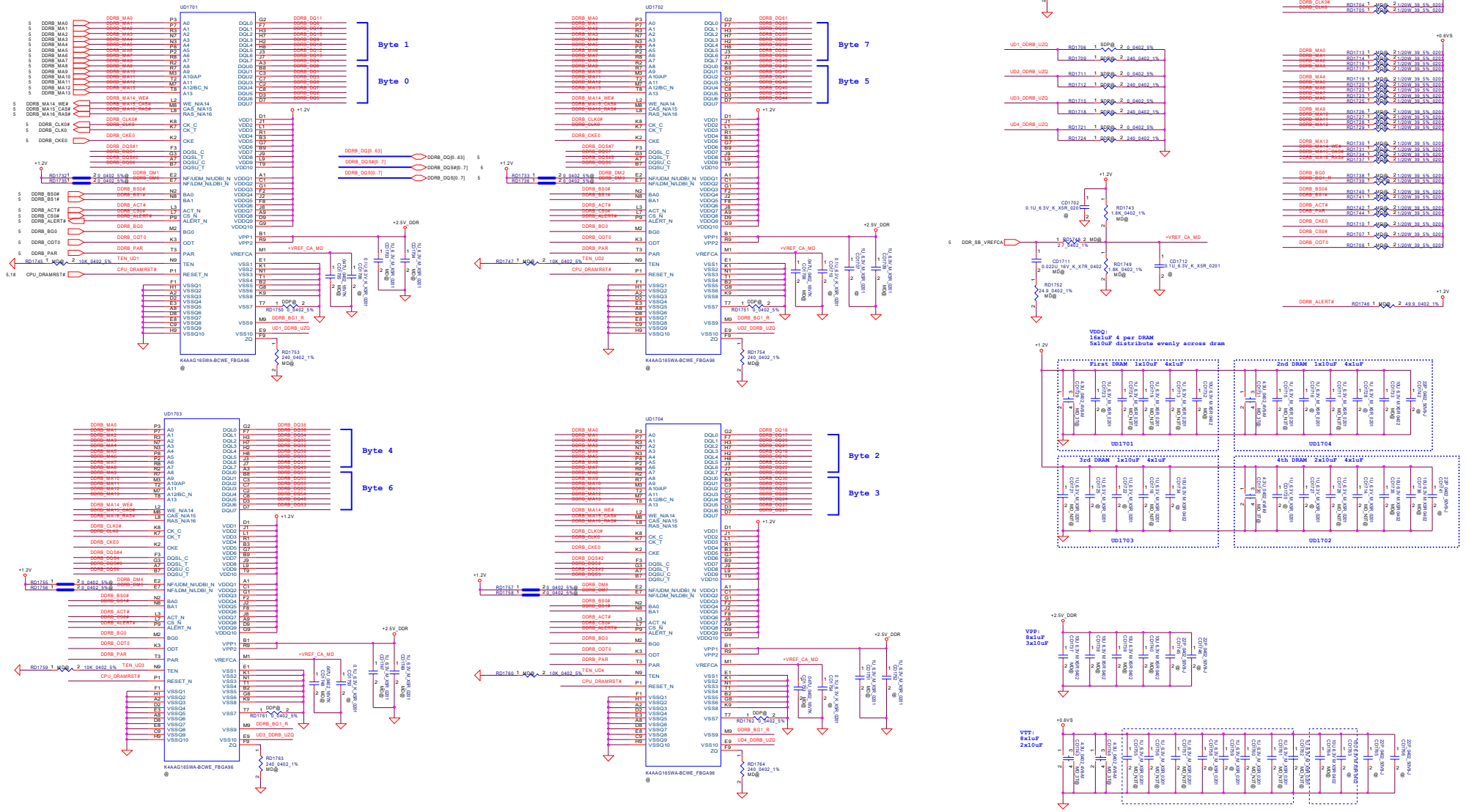


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Title: DDR4 Memory Down

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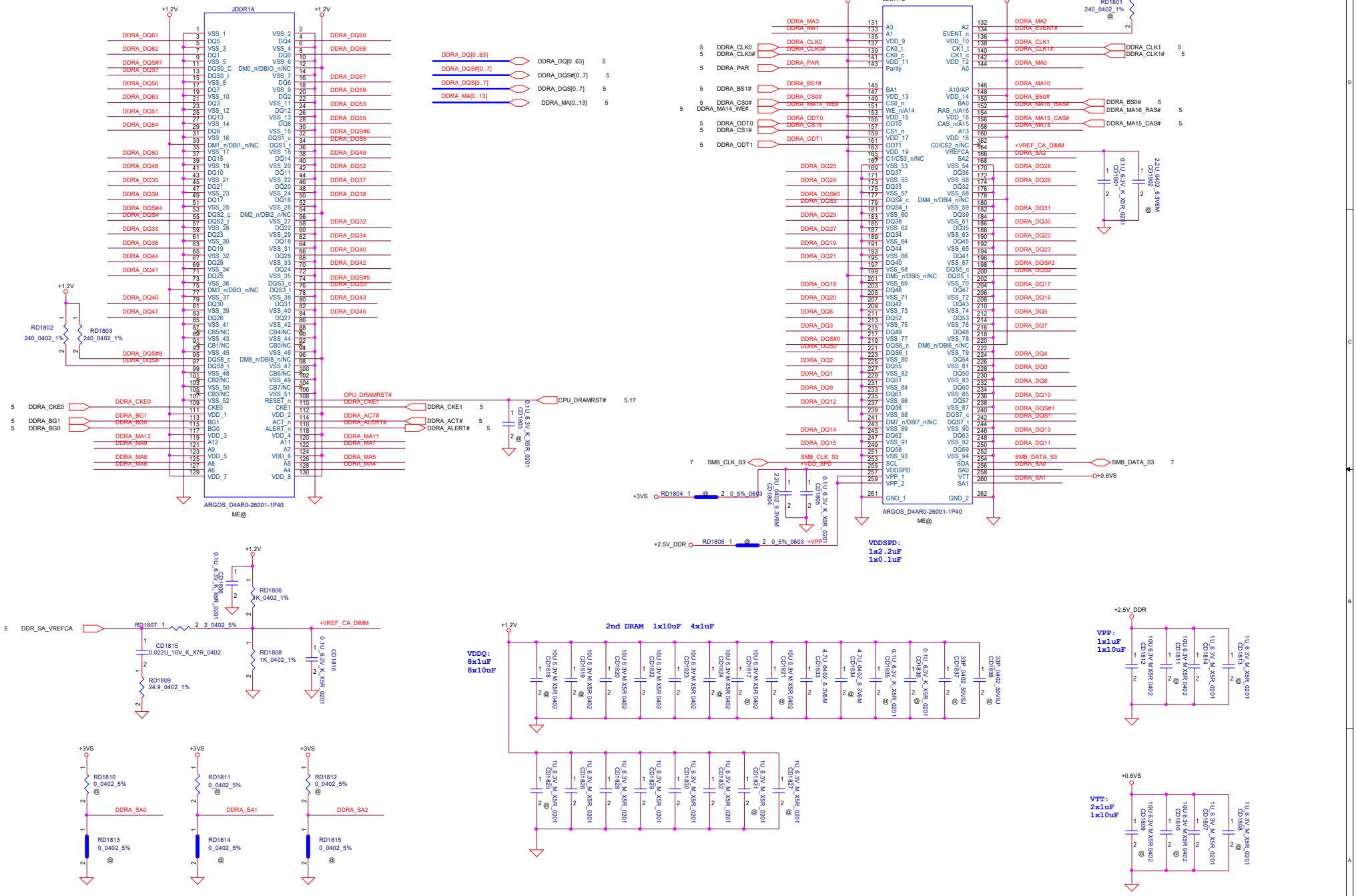


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Title: DDR4 SO-DIMM

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## N16x GPIO

| GPIO | I/O | ACTIVE | Function Description |
|---|---|---|---|
| GPIO0 | OUT | - | GPU Core VDD PWM control signal |
| GPIO1 | OUT | N/A | FB Enable for GC6 2.0 |
| GPIO2 | OUT | N/A | |
| GPIO3 | OUT | N/A | |
| GPIO4 | OUT | N/A | |
| GPIO5 | OUT | N/A | GPU power sequencing---3V3_MAIN_EN |
| GPIO6 | IN | - | GPU wake signal for GC6 2.0 |
| GPIO7 | OUT | N/A | |
| GPIO8 | I/O | - | System side PCIe reset Monitor |
| GPIO9 | I/O | N/A | 2.2K Pull-up |
| GPIO10 | OUT | | FBVREF_ALTV for GDDR5 |
| GPIO11 | OUT | - | |
| GPIO12 | IN | | AC Power Detect Input (10K pull High) |
| GPIO13 | OUT | - | Phase Shedding |
| GPIO14 | IN | N/A | |
| GPIO15 | IN | N/A | |
| GPIO16 | | N/A | |
| GPIO17 | IN | N/A | |
| GPIO18 | IN | N/A | |
| GPIO19 | IN | N/A | |
| GPIO20 | | N/A | |
| GPIO21 | OUT | | GPU PCIe self-reset control |
| OVERT | OUT | | Active Low Thermal Catastrophic Over Temperature |

## Performance Mode P0 TDP and EDP-Continuous current (GDDR5)

| | GPU | Mem | Min Core Clk | NVVDD | | | FBVDD (1.35V) | | FBVDDQ (GPU+Mem) (1.35V) | | (1.05V) (6) | | Other (3.3V) | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Products | (W) | (W) | (MHz) | (V) | (A) | (W) | (A) | (W) | (A) | (W) | (mA) | (W) | (mA) | (W) |
| N16S-GMR | 16 | 1.6 | 849 | TBD | 19 | TBD | 2 | TBD | 4.2 | TBD | 800 | TBD | 60 | TBD |
| N16S-GTR | 18 | 1.7 | 967 | | 26.5 | | 2 | | 4.2 | | 800 | | 60 | |

## N16x Multi-level Straps

| Physical Strapping pin | Power Rail | Logical Strapping Bit3 | Logical Strapping Bit2 | Logical Strapping Bit1 | Logical Strapping Bit0 |
|---|---|---|---|---|---|
| ROM_SCLK | +3VGS | SOR3_EXPOSED | SOR2_EXPOSED | SOR1_EXPOSED | SOR0_EXPOSED |
| ROM_SI | +3VGS | RAM_CFG[3] | RAM_CFG[2] | RAM_CFG[1] | RAM_CFG[0] |
| ROM_SO | +3VGS | DEVID_SEL | PCIE_CFG | SMB_ALT_ADDR | VGA_DEVICE |
| STRAP0 | +3VGS | Reserved(keep pull-up and pull-down footprint and stuff 50Kohm pull-up) | | | |
| STRAP1 | +3VGS | Reserved(keep pull-up and pull-down footprint and not stuff by default) | | | |
| STRAP2 | +3VGS | | | | |
| STRAP3 | +3VGS | | | | |
| STRAP4 | +3VGS | | | | |

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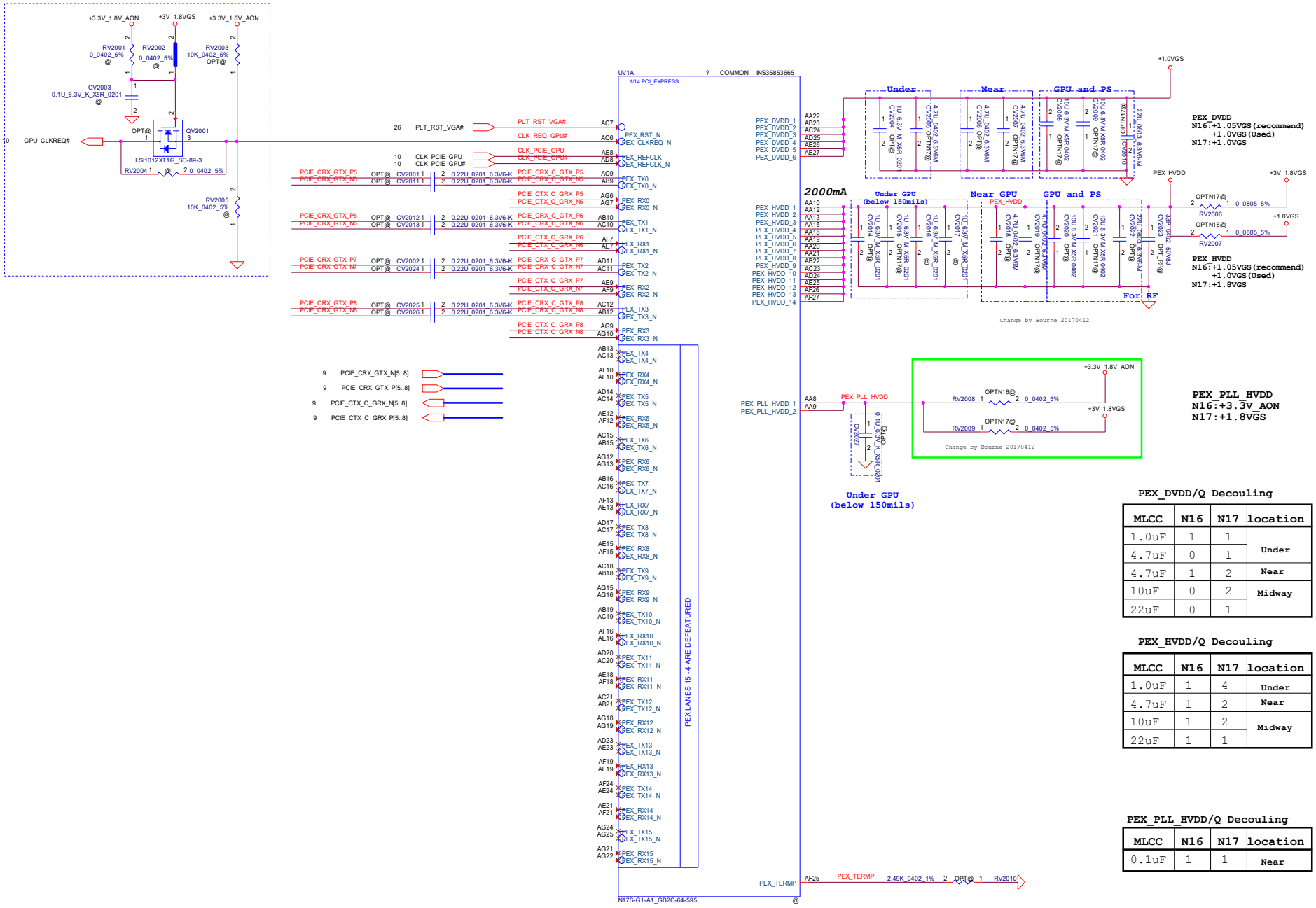


## PEX_DVDD/Q Decouling

| MLCC | N16 | N17 | location |
|---|---|---|---|
| 1.0uF | 1 | 1 | Under |
| 4.7uF | 0 | 1 | |
| 4.7uF | 1 | 2 | Near |
| 10uF | 0 | 2 | Midway |
| 22uF | 0 | 1 | |

## PEX_HVDD/Q Decouling

| MLCC | N16 | N17 | location |
|---|---|---|---|
| 1.0uF | 1 | 4 | Under |
| 4.7uF | 1 | 2 | Near |
| 10uF | 1 | 2 | Midway |
| 22uF | 1 | 1 | |

## PEX_PLL_HVDD/Q Decouling

| MLCC | N16 | N17 | location |
|---|---|---|---|
| 0.1uF | 1 | 1 | Near |

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Title: GPU_PCIE Interface

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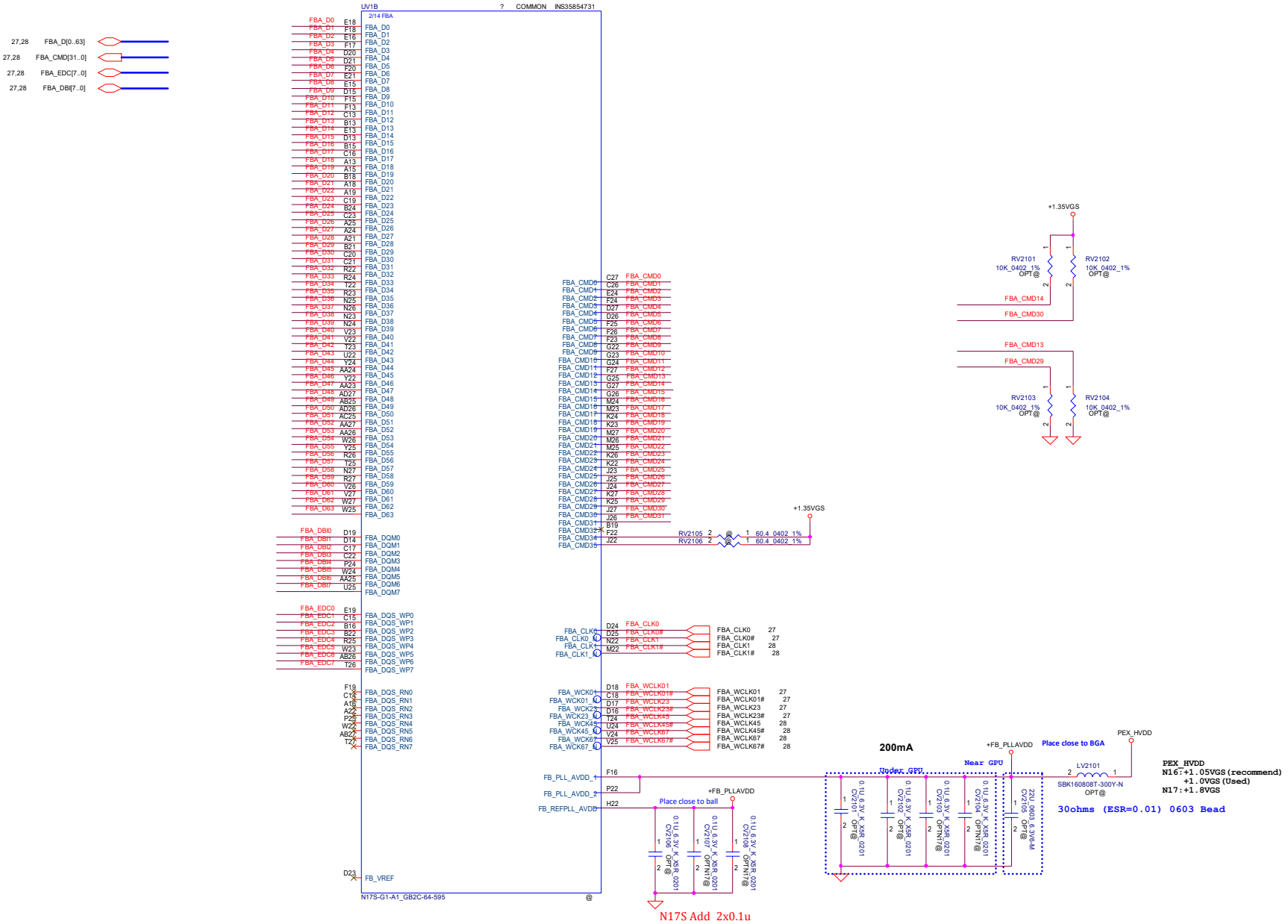


**FB_PLL/Q Decouling**

| MLCC | N16 | N17 | location |
|---|---|---|---|
| 0.1uF | 2 | 4 | Under |
| 22uF | 1 | 1 | Near |

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Title: GPU_MEM Interface

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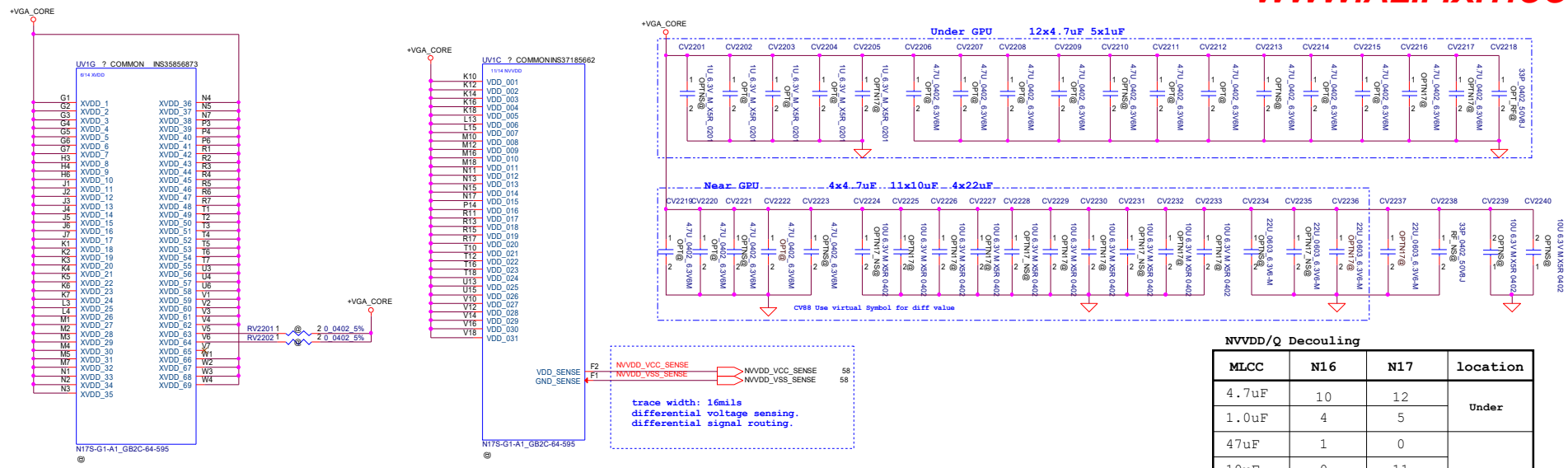
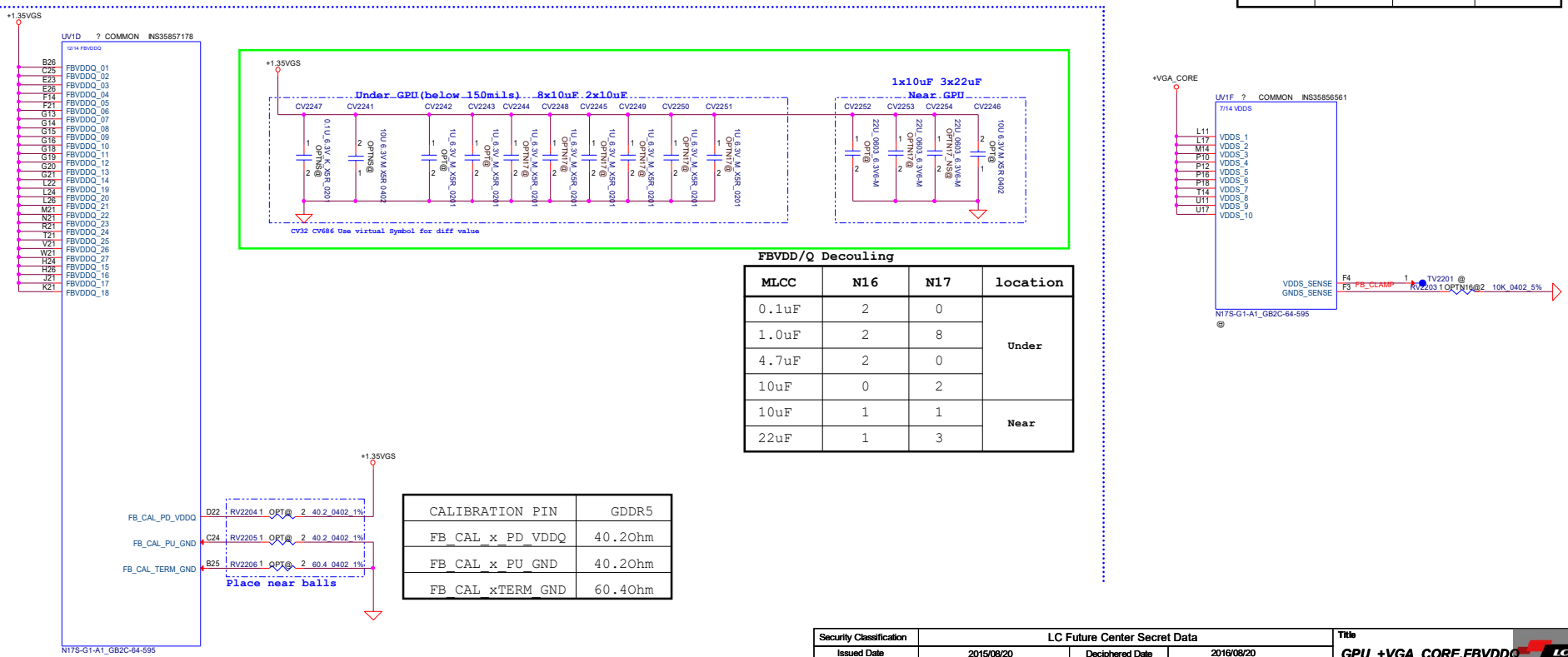



**NVVDD/Q Decouling**

| MLCC | N16 | N17 | location |
|---|---|---|---|
| 4.7uF | 10 | 12 | Under |
| 1.0uF | 4 | 5 | |
| 47uF | 1 | 0 | Near |
| 10uF | 0 | 11 | |
| 22uF | 1 | 4 | |
| 4.7uF | 5 | 4 | |
| 330uF | 1 | 2 | |




**FBVDDQ Decouling**

| MLCC | N16 | N17 | location |
|---|---|---|---|
| 0.1uF | 2 | 0 | Under |
| 1.0uF | 2 | 8 | |
| 4.7uF | 2 | 0 | |
| 10uF | 0 | 2 | |
| 10uF | 1 | 1 | Near |
| 22uF | 1 | 3 | |

| CALIBRATION PIN | GDDR5 |
|---|---|
| FB_CAL_x_PD_VDDQ | 40.2Ohm |
| FB_CAL_x_PU_GND | 40.2Ohm |
| FB_CAL_xTERM_GND | 60.4Ohm |

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Title: GPU_+VGA_CORE,FBVDDQ

Size: C | Document Number: GS44D/GS54D | Rev: 0.1

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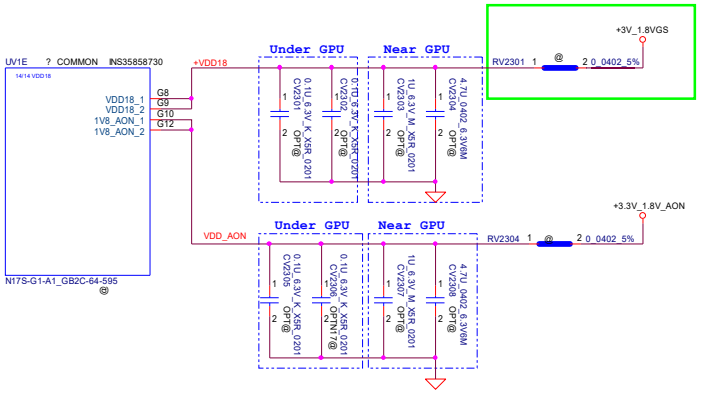


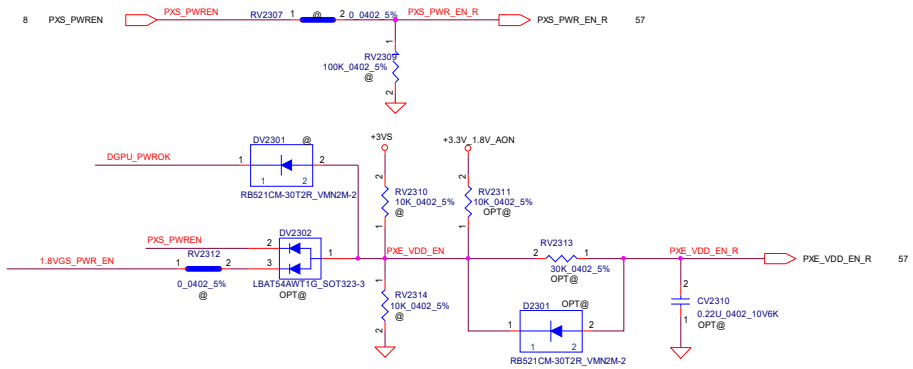

## N16 3V3_MAIN(N17 VDD_18) Decouling

| MLCC | N16 | N17 | location |
|---|---|---|---|
| 0.1uF | 2 | 2 | Under |
| 1.0uF | 1 | 1 | Near |
| 4.7uF | 1 | 1 | |

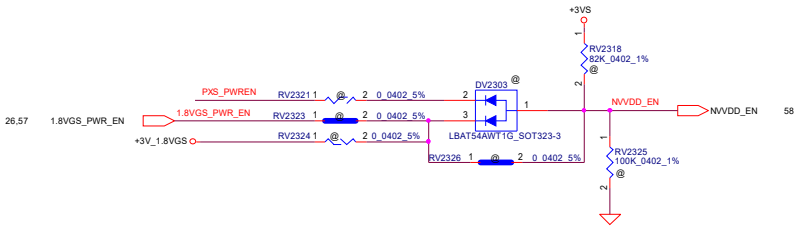
## N16 3V3_AON(N17 1V8_AON) Decouling

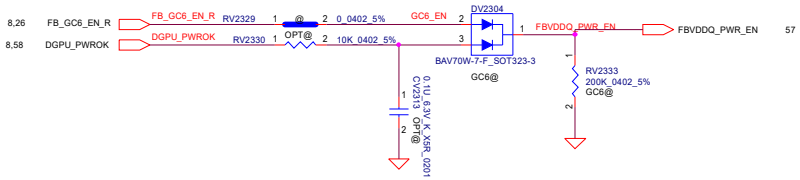
| MLCC | N16 | N17 | location |
|---|---|---|---|
| 0.1uF | 1 | 2 | Under |
| 1.0uF | 1 | 1 | Near |
| 4.7uF | 1 | 1 | |

## PXE_VDD & 1V8_AON

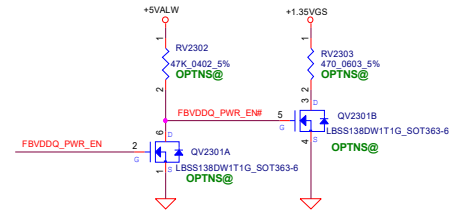


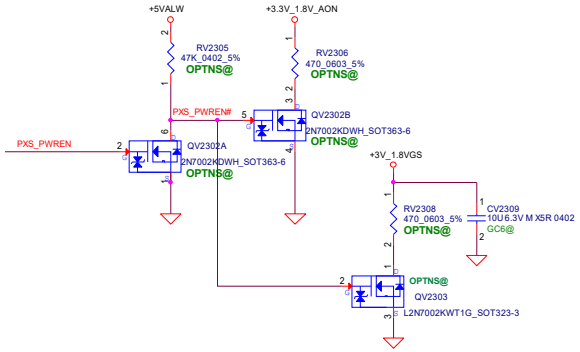

## +1.8VG_AON TO +1.8VGS



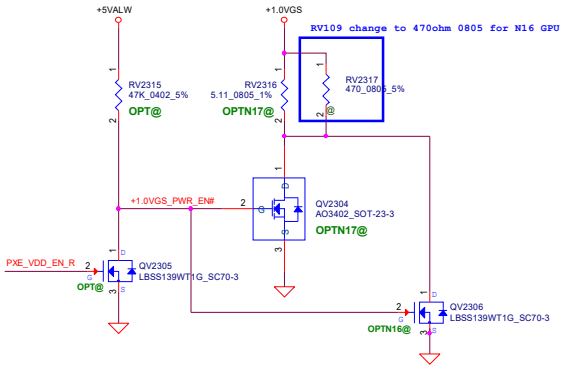



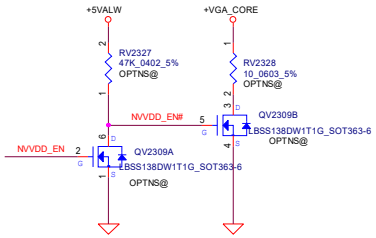

Discharge




RV2316 建虚拟料号,N16=470 ohm,N17=5.11 ohm

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Title: GPU_AON/MAIN PWR/SEQUE

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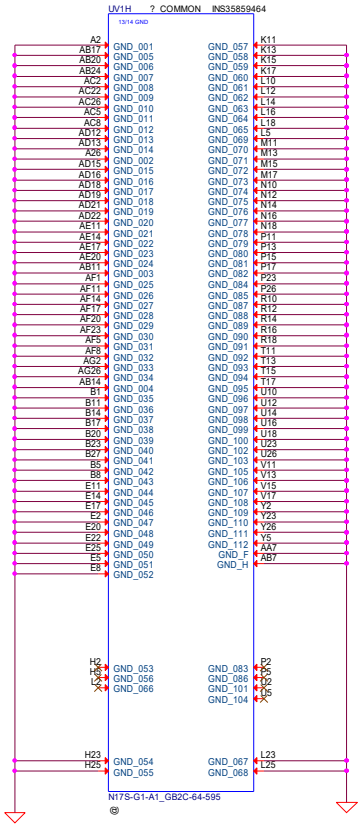


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Title: GPU_GND

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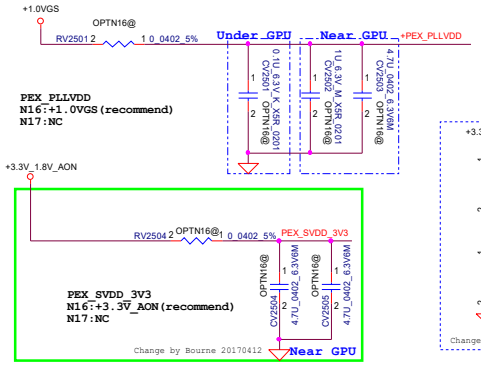
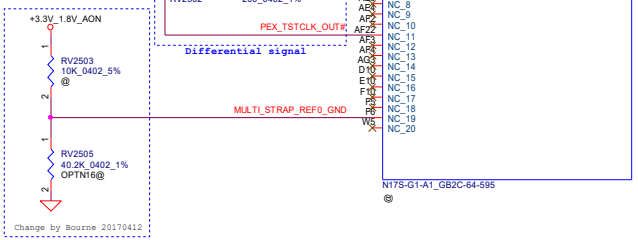
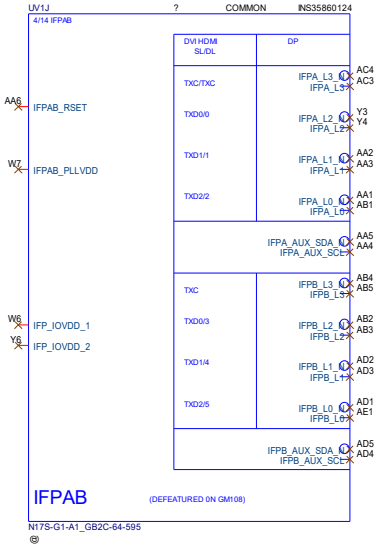
### PEX_PLLVDD/Q Decouling

| MLCC | N16 | N17 | location |
|---|---|---|---|
| 1.0uF | 1 | NA | Under |
| 1uF | 1 | NA | Near |
| 4.7uF | 1 | NA | |

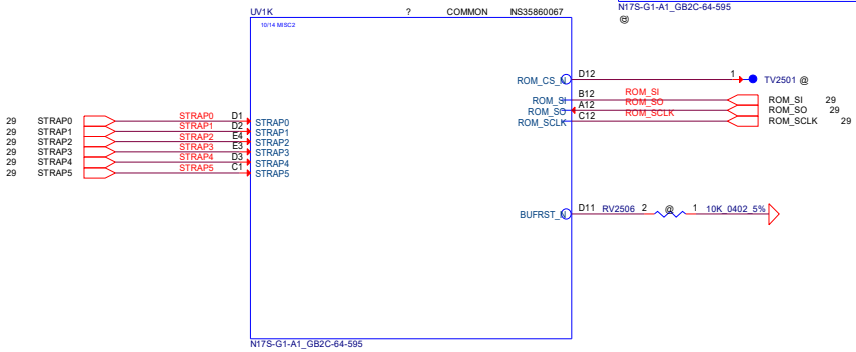


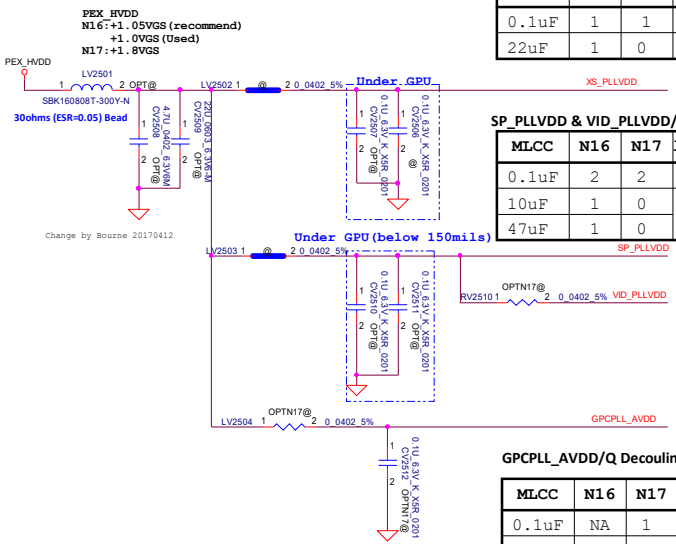

### PEX_SVDD/Q Decouling

| MLCC | N16 | N17 | location |
|---|---|---|---|
| 4.7uF | 2 | NA | Near |



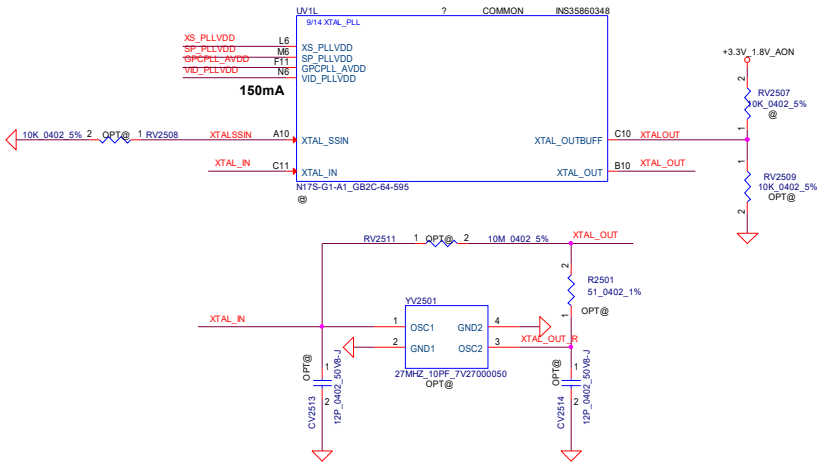

### XS_PLLVDD/Q Decouling

| MLCC | N16 | N17 | location |
|---|---|---|---|
| 0.1uF | 1 | 1 | Under |
| 22uF | 1 | 0 | Near |




### SP_PLLVDD & VID_PLLVDD/Q Decouling

| MLCC | N16 | N17 | location |
|---|---|---|---|
| 0.1uF | 2 | 2 | Under |
| 10uF | 1 | 0 | Near |
| 47uF | 1 | 0 | |




### GPCPLL_AVDD/Q Decouling

| MLCC | N16 | N17 | location |
|---|---|---|---|
| 0.1uF | NA | 1 | Under |
| 4.7uF | NA | 1 | Near |
| 22uF | NA | 1 | |

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Title: GPU_STRAP/DP/HDMI

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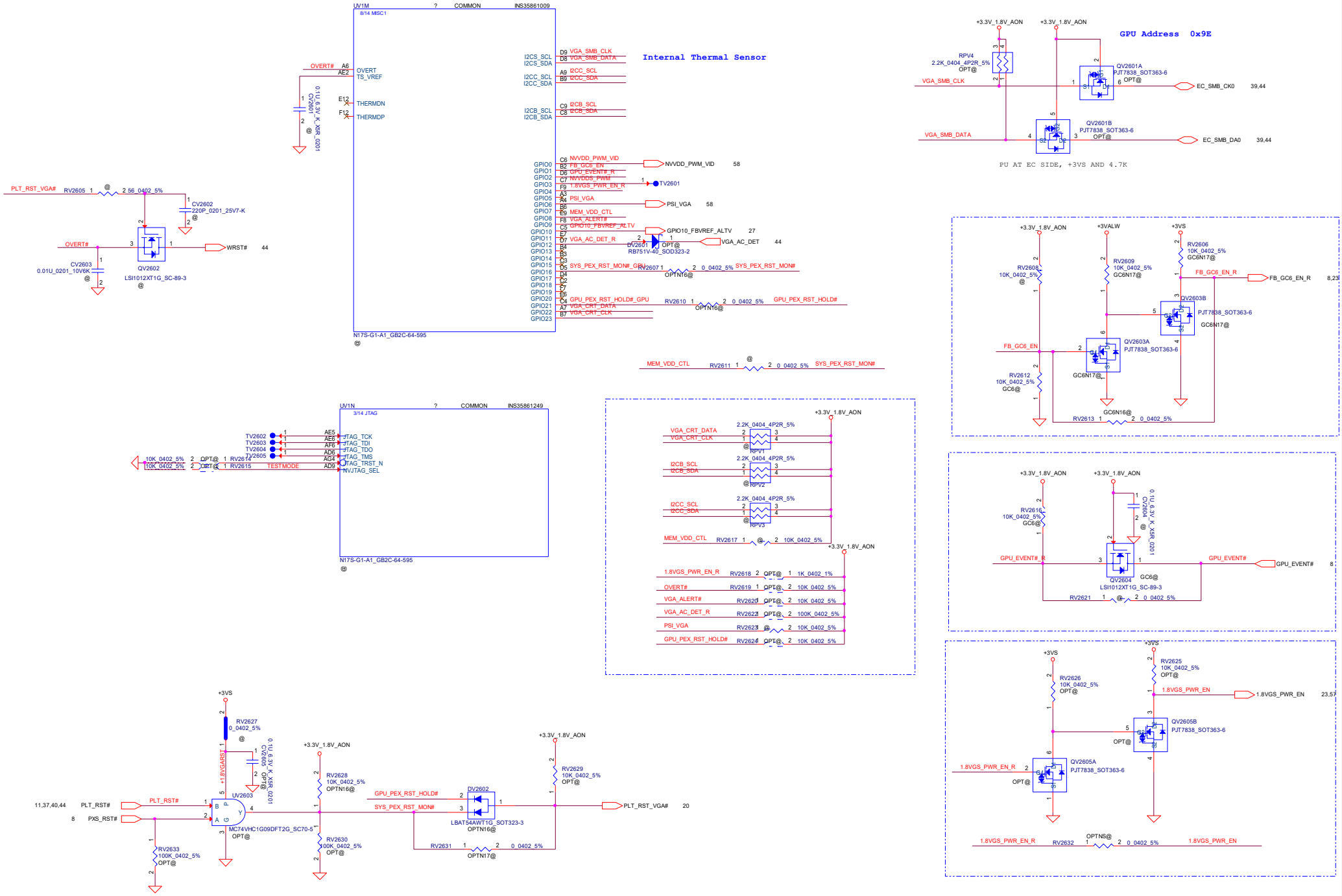


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Title: GPU_GPIO/JTAG

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Lower 32 bits

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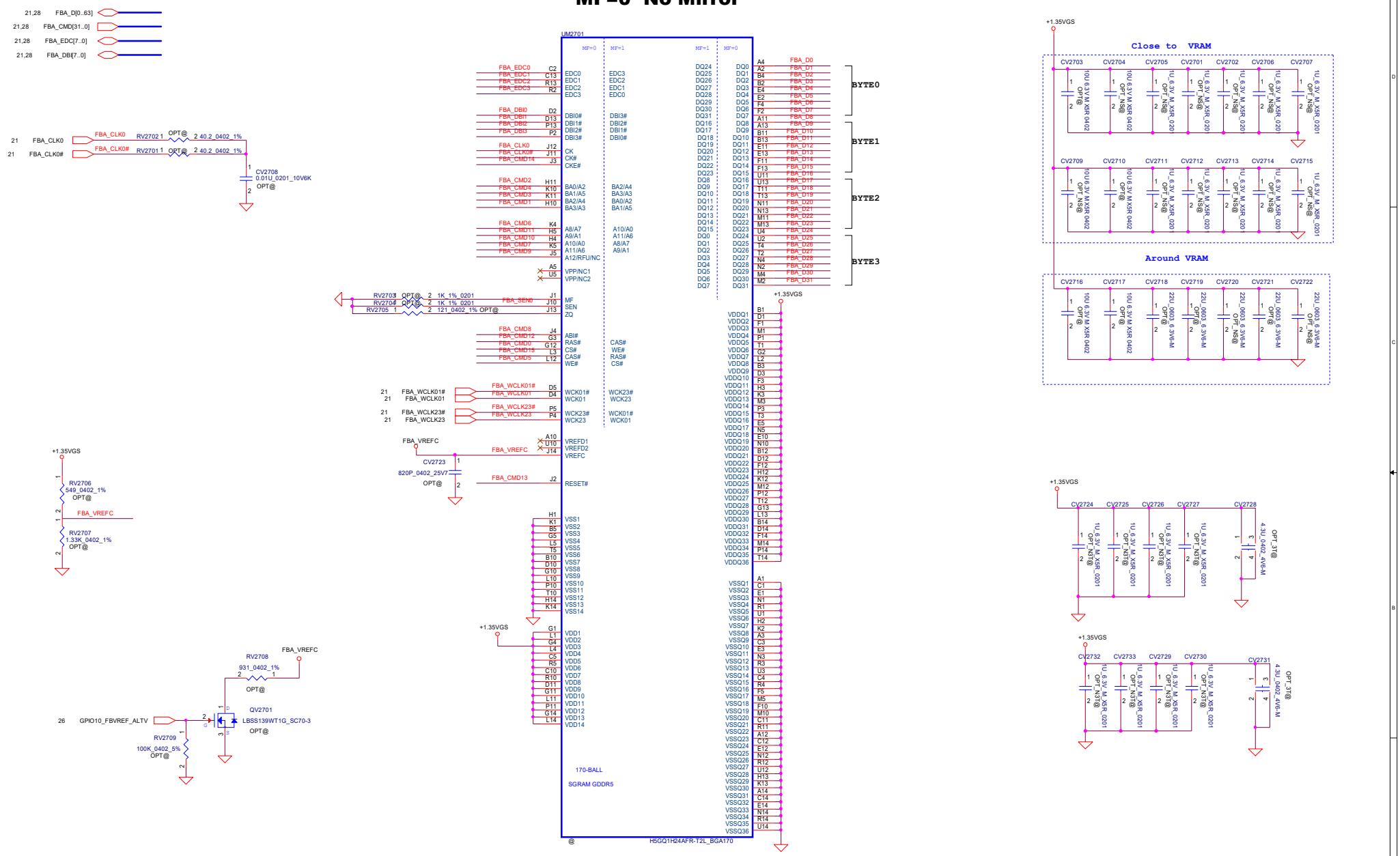
# MF=0 No Mirror

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Title: GPU_GDDR5_Rank0_[31:0]

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upper 32 bits

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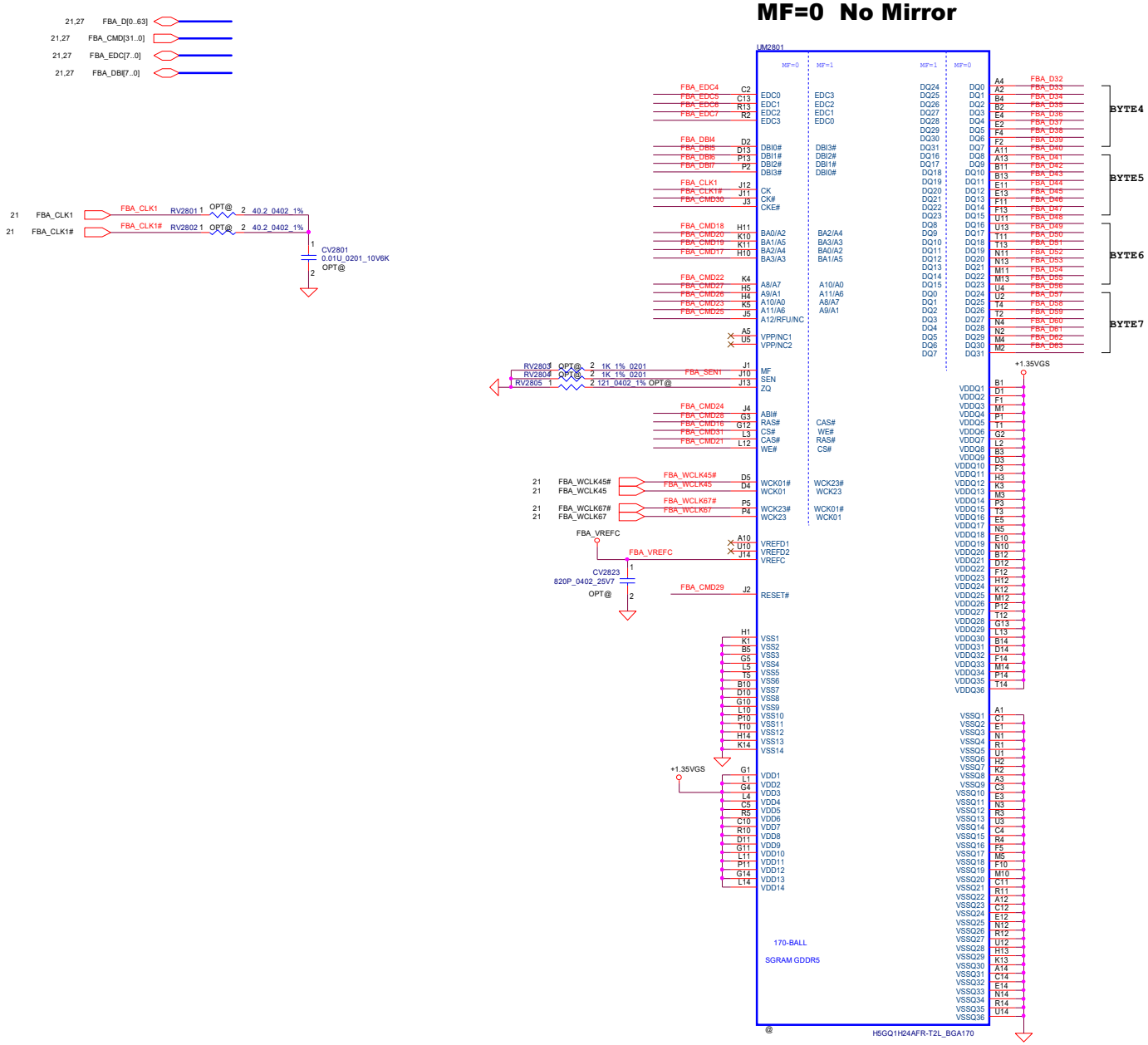
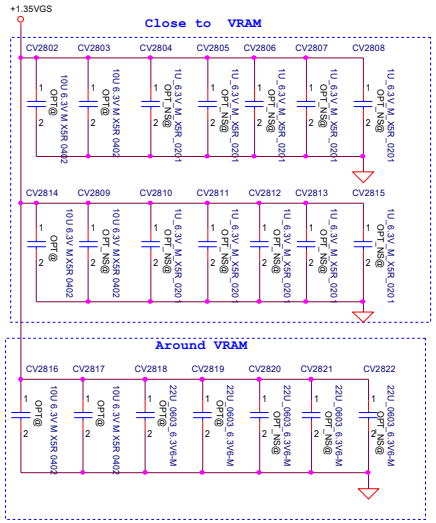
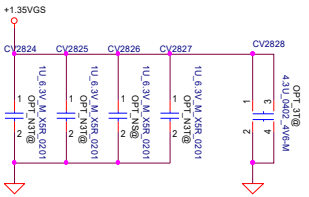
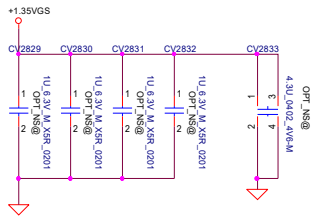
# MF=0 No Mirror

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Title: GPU_GDDR5_Rank0_[64:32]

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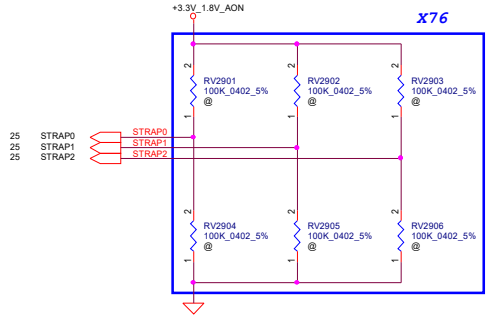
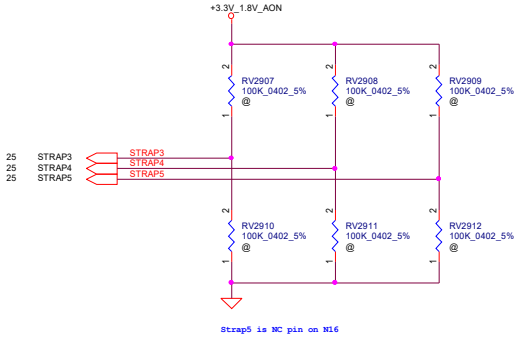



| GPU | FB Memory (GDDR5) | | RAMCFG[4:0] | STRAP2 | STRAP1 | STRAP0 |
|---|---|---|---|---|---|---|
| 8Gb | Samsung 8Gb | K4G80325FB-HC28 | 0(0x0000) | L | L | L |
| | Micron 8Gb | MT51J256M32HF-70:A | 1(0x0001) | L | L | H |
| | Hynix 8Gb | H5GC8H24MJR-R0C | 2(0x0010) | L | H | L |
| | | | | | | |
| | | | | | | |
| | | | | | | |



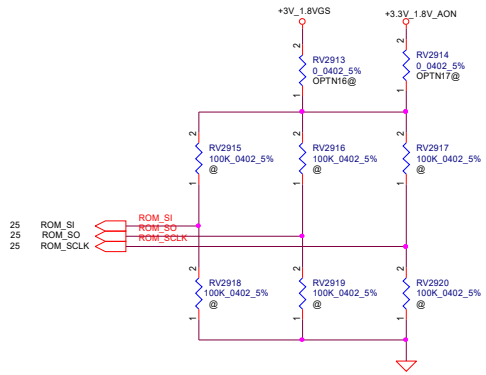

| STRAP5 | STRAP4 | STRAP3 | SMB_ALT_ADDR | DEVID_SEL | PCIE_CFG | VGA_DEVICE |
|---|---|---|---|---|---|---|
| L | L | L | 0 | 0 | 0 | 0 |

1: SMB_ALT_ADDR ENABLE
0: SMB_ALT_ADDR DISABLE

1: DEVID_SEL REBRAND
0: DEVID_SEL ORIGNAL

1: PCIE_CFG LOW POWER
0: PCIE_CFG HIGH POWER

1: VGA_DEVICE ENABLE
0: VGA_DEVICE DISABLE




| | ROM_SO | ROM_SI | ROM_SCLK | SOR_EXPOSED[3:0] |
|---|---|---|---|---|
| N17S-G1 | H | H | M | 0000 |
| N16S-GTR | | | | |

1:ENABLE 0:DISABLE

SOR0/1/2/3 DISABLE

| DEVID_SEL | |
|---|---|
| 0 | (Default) |
| 1 | |

| PCIE_CFG | |
|---|---|
| 0 | (Default) |
| 1 | |

| SMBUS_ALT_ADDR | |
|---|---|
| 0 | 0x9E (Default) |
| 1 | 0x9C (Multi-GPU usage) |

| VGA_DEVICE | |
|---|---|
| 0 | 3D Device (Class Code 302h) |
| 1 | VGA Device (Default) |

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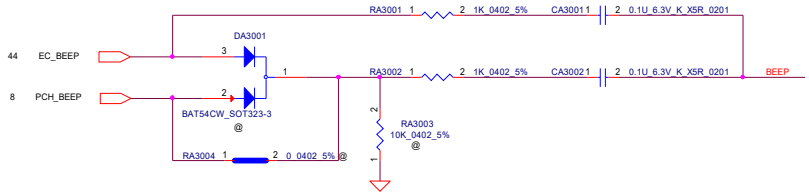
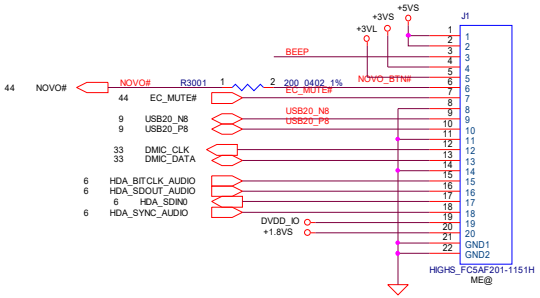
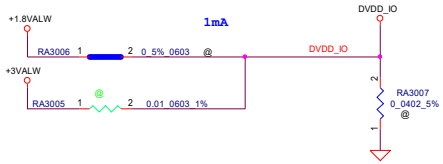
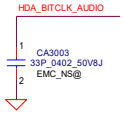
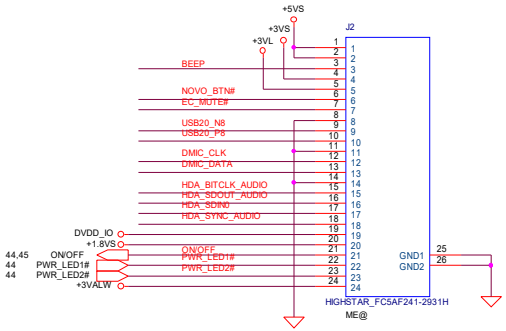


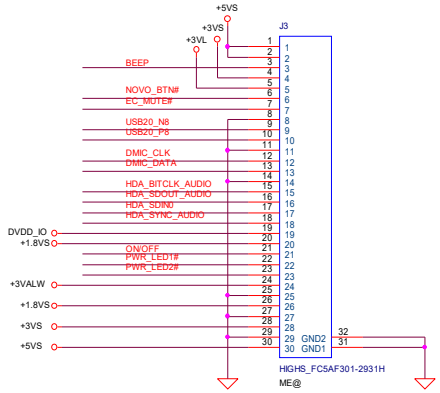




**CPU HDA BUS power 1.8VALW**

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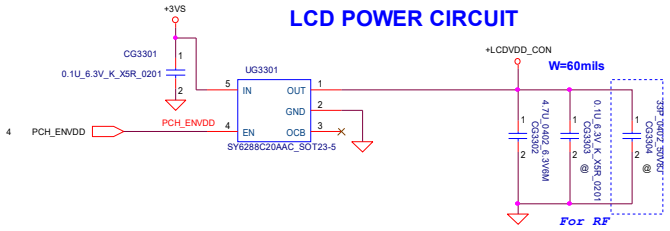
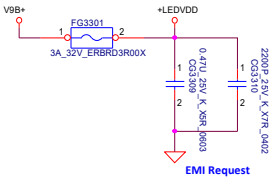
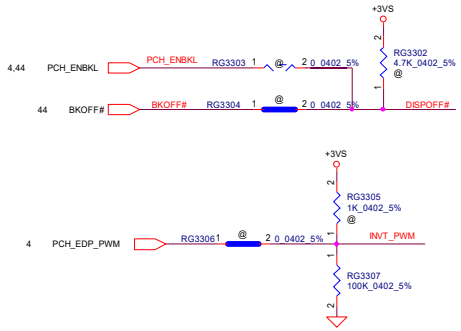
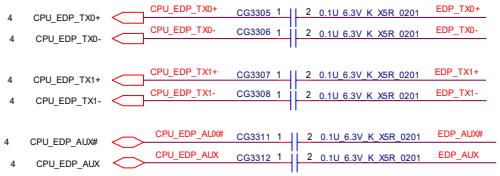
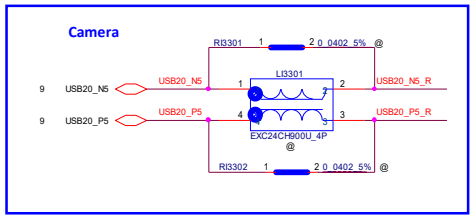
## LCD POWER CIRCUIT

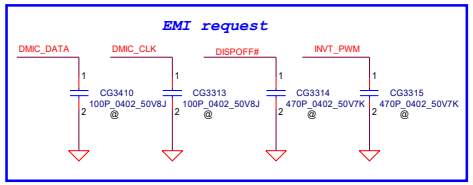
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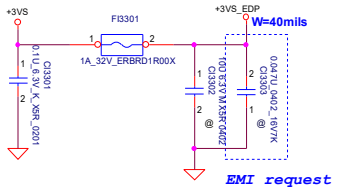


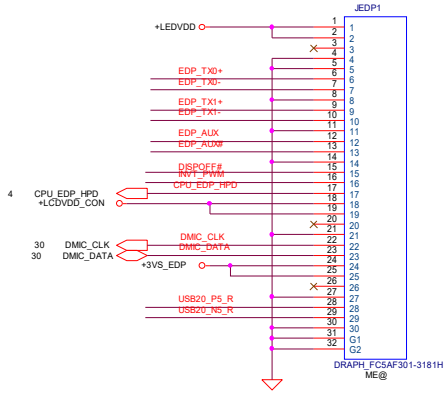


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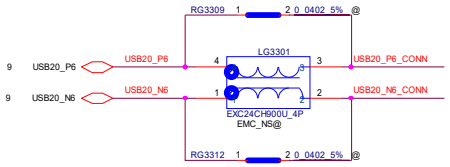
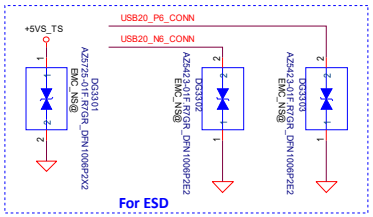
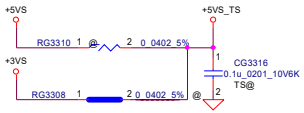
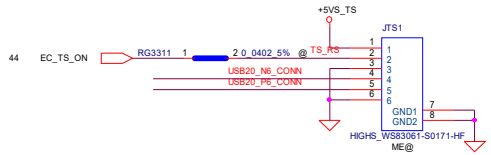



For EMI

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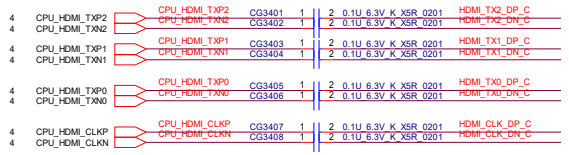
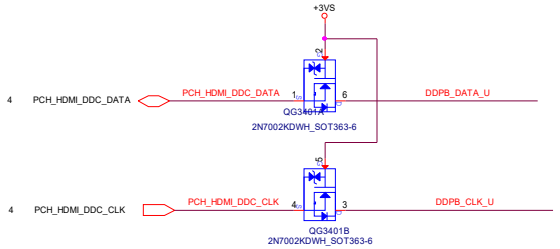
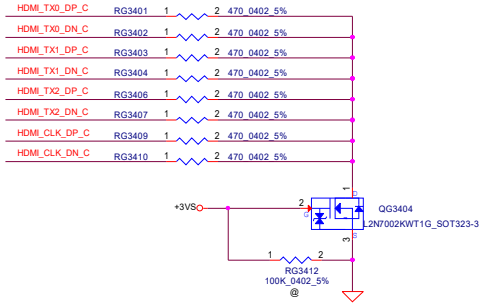
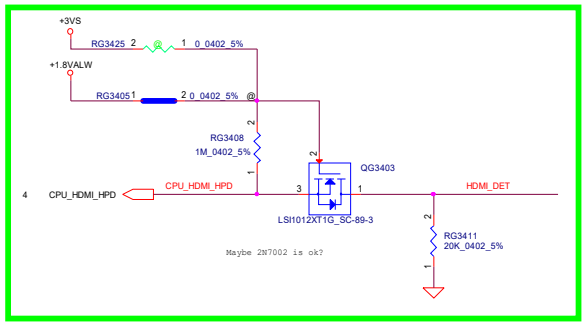
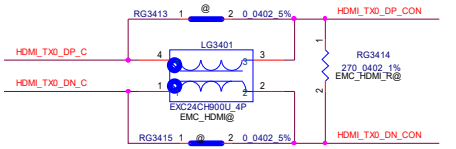


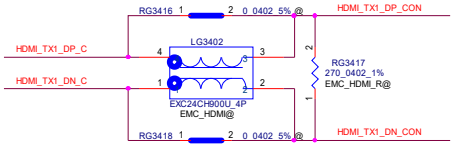



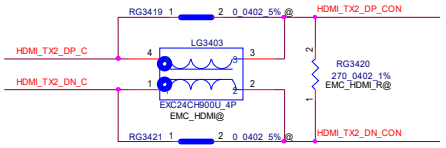

**Need to change about 470Ohm 5%-575412 Page115 Rev0.8**

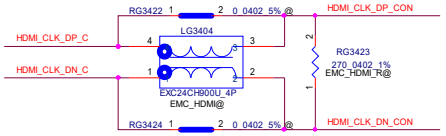
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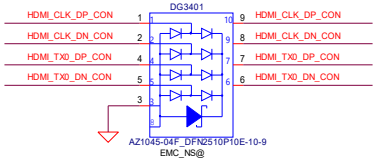


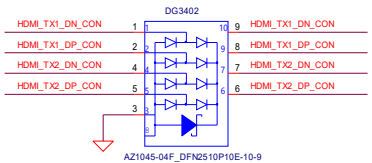


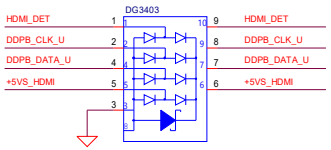


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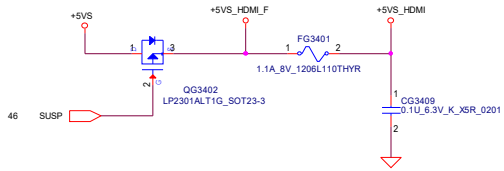


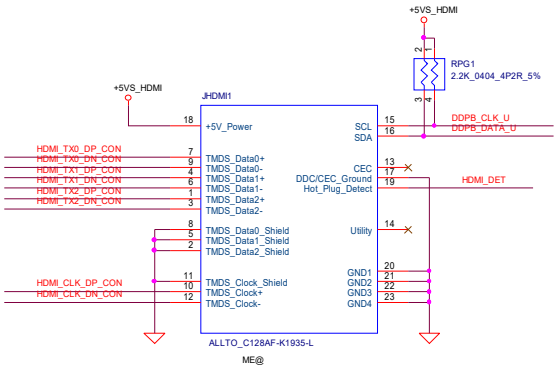


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**HALL Sensor**

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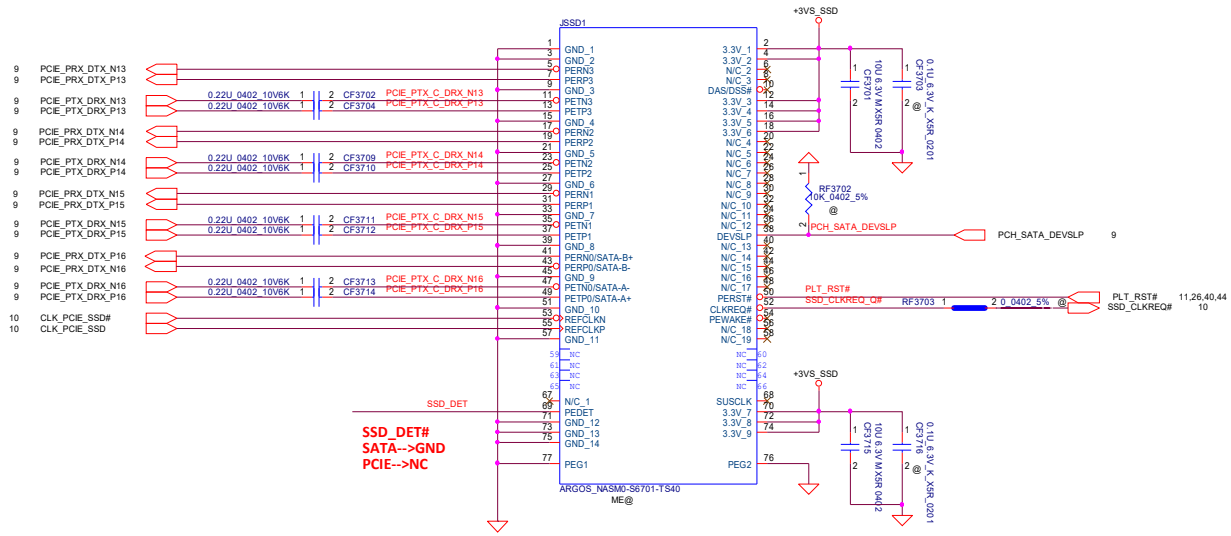
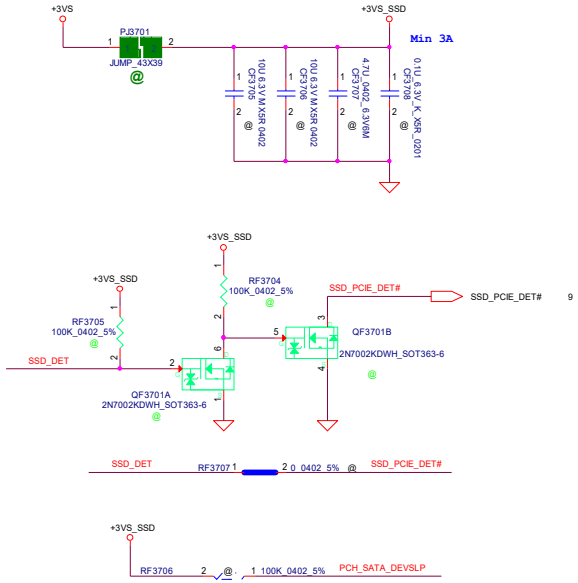
## M.2 SSD

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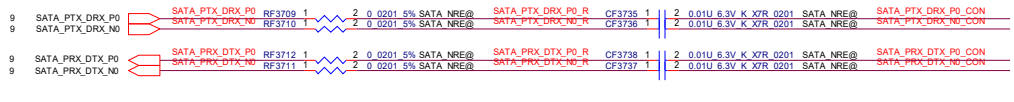


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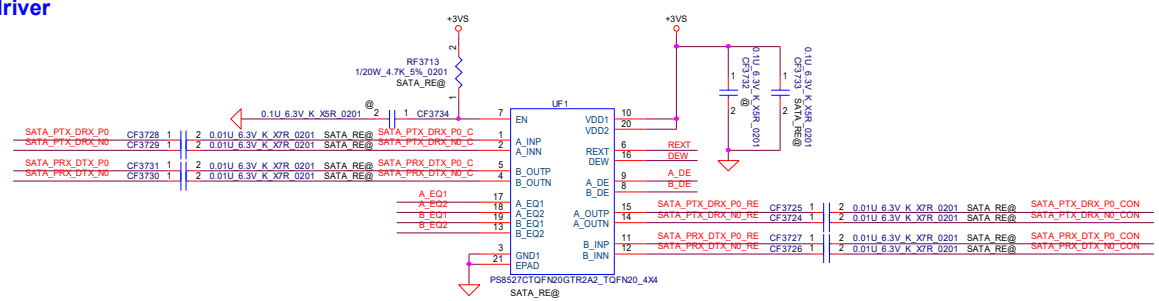


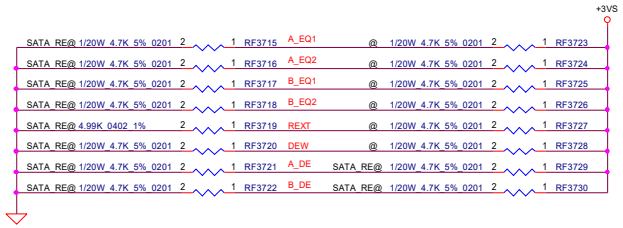


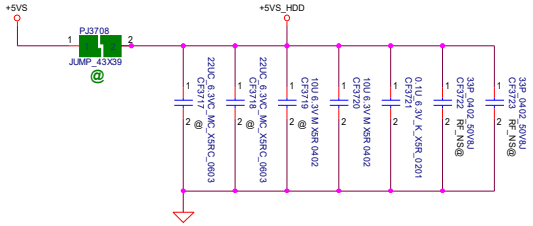


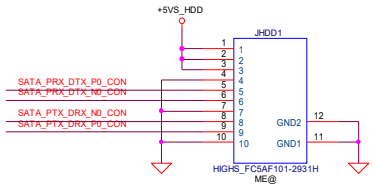


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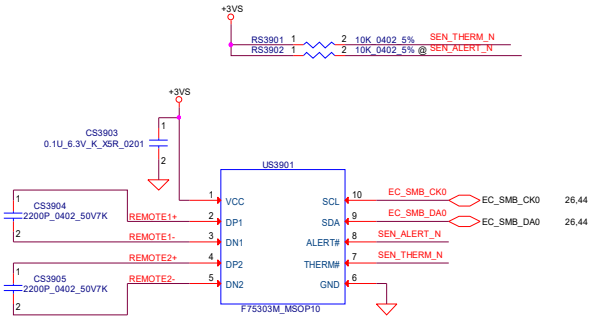
## SMSC thermal sensor




**REMOTE1+/-, REMOTE2+/-:**
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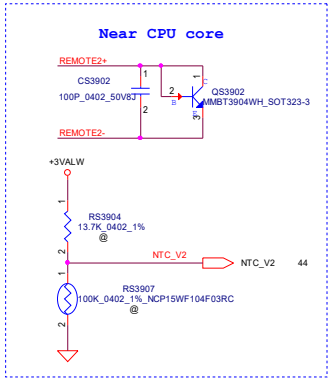
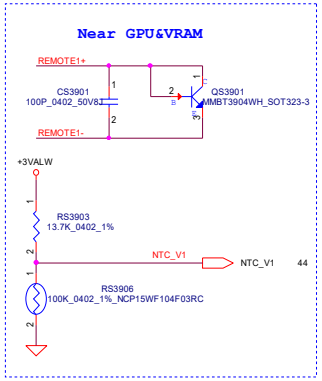
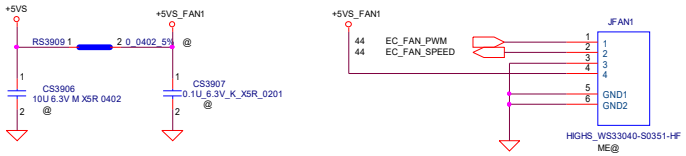



## FAN Conn

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# Mini-Express Card(WLAN/WiMAX)

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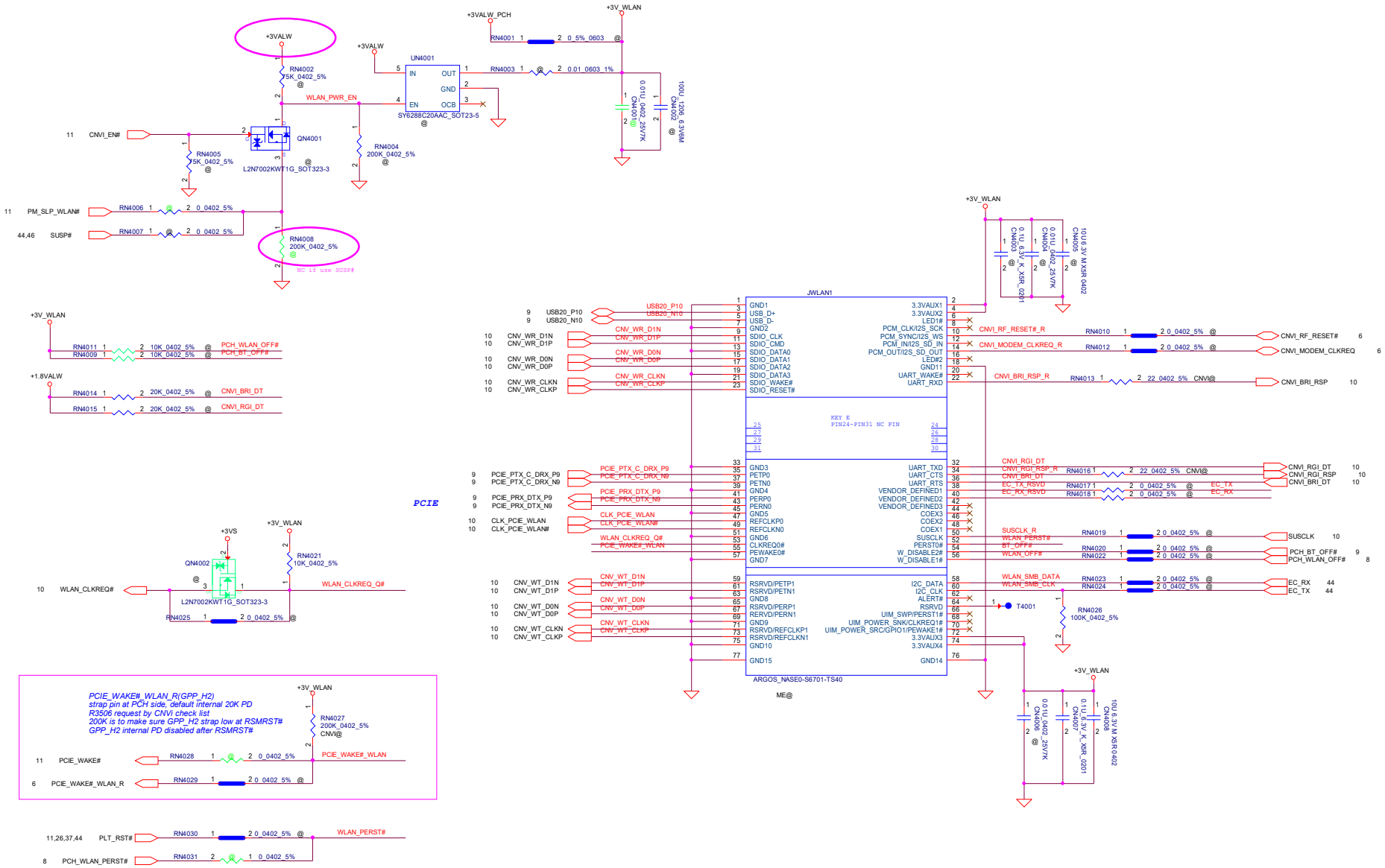


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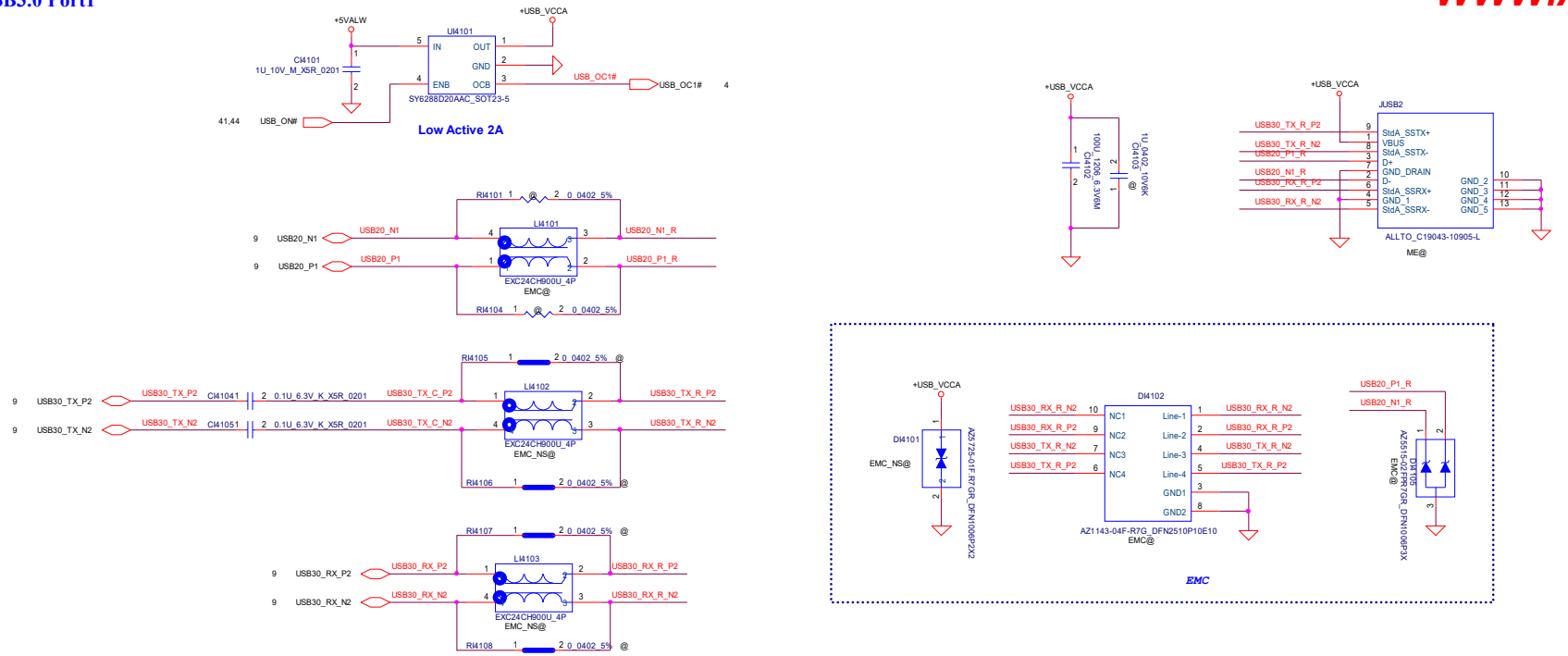
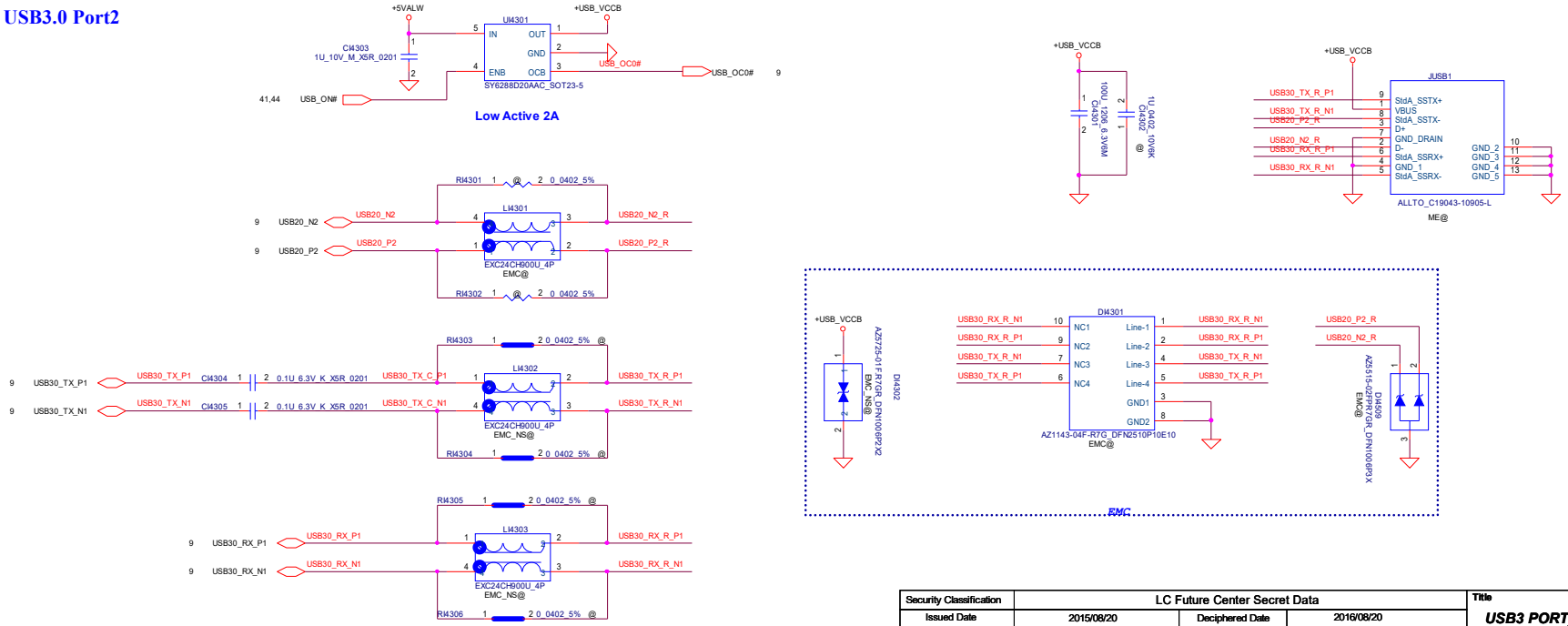
## USB3.0 Port1




## USB3.0 Port2

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Title: USB3 PORT_LEFT

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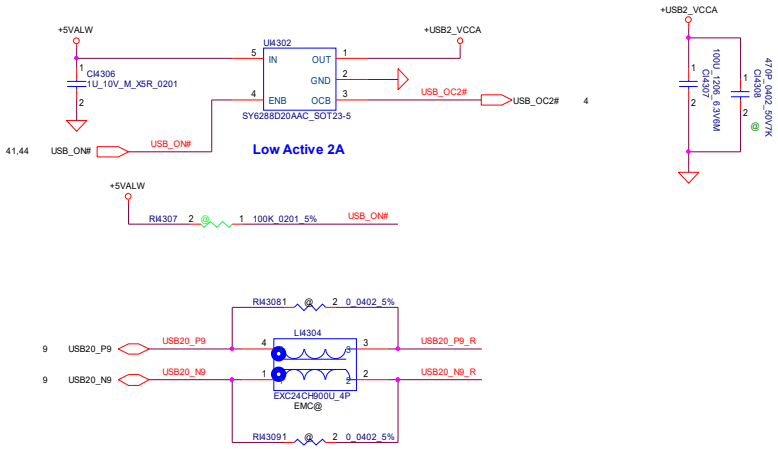
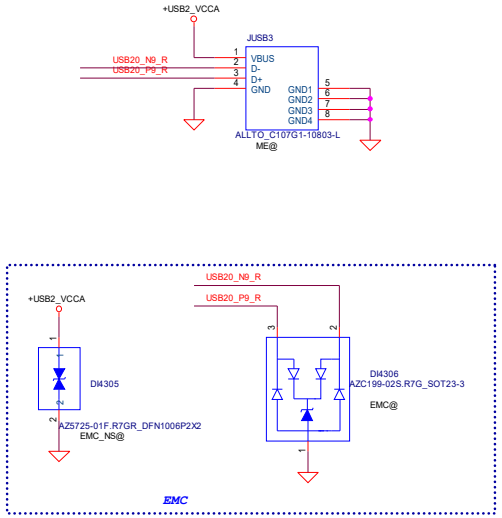
## USB2.0 PORT x1

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Title: USB3 Port_Right & USB2.0

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Title

**Blank**

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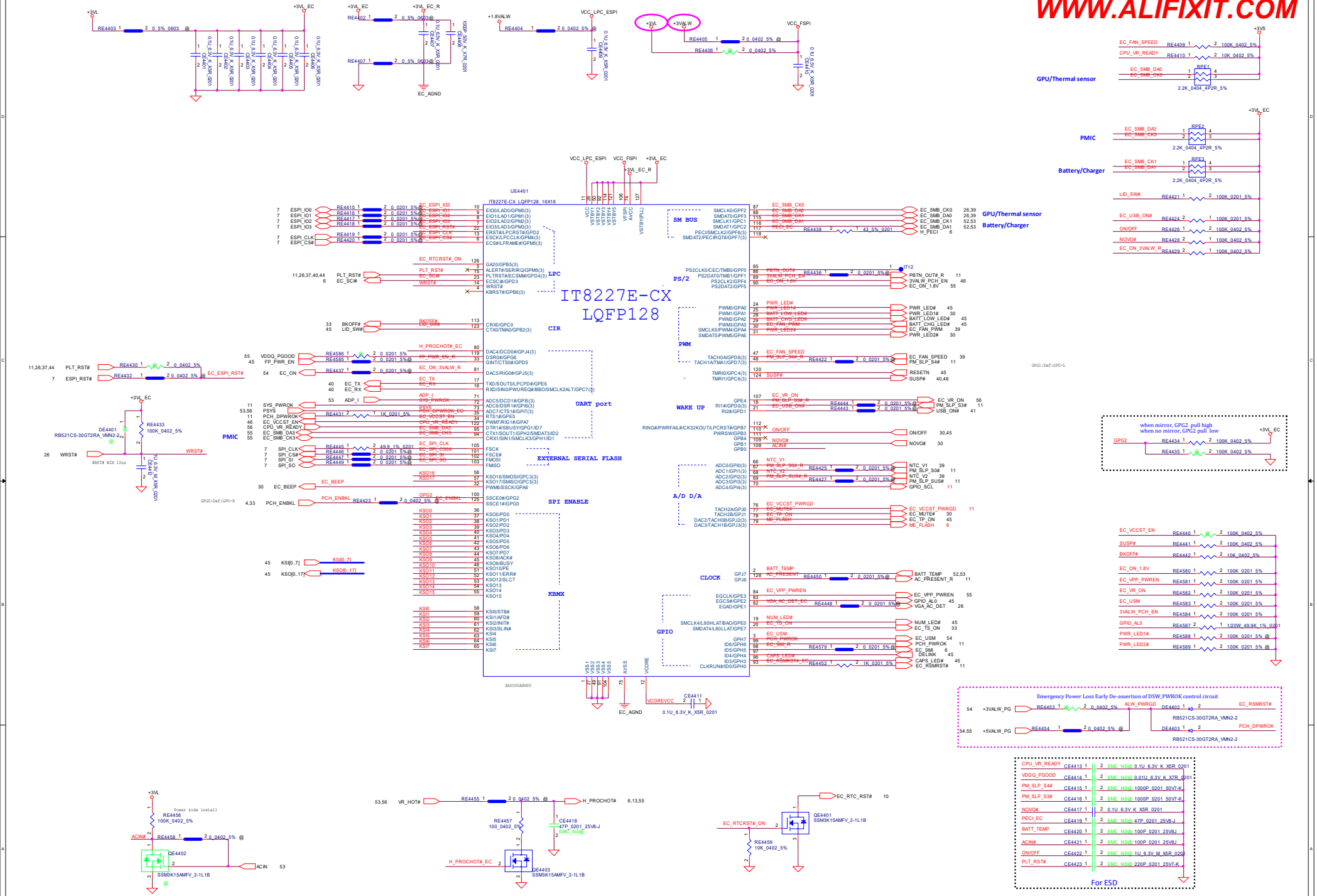


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Title: EC ITE8586LQFP

Size: Custom | Document Number: GS44D/GS54D | Rev: 0.1

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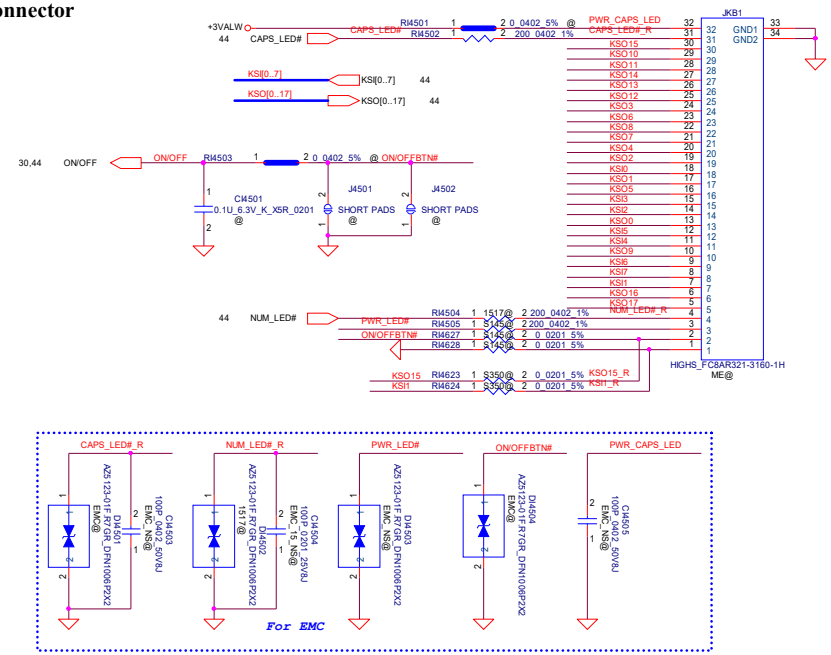
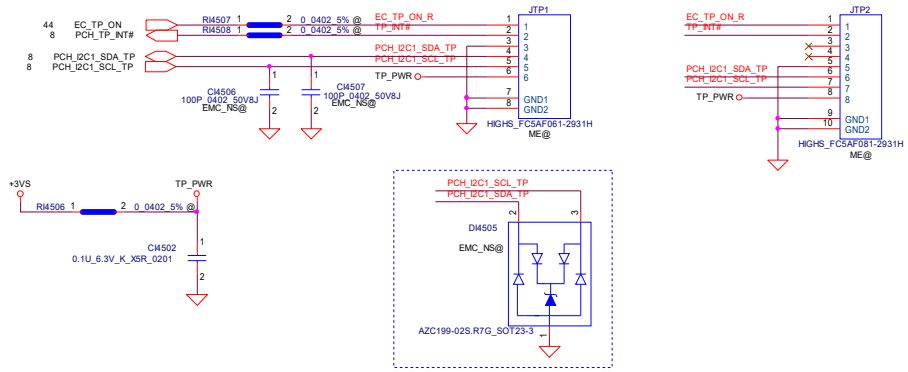
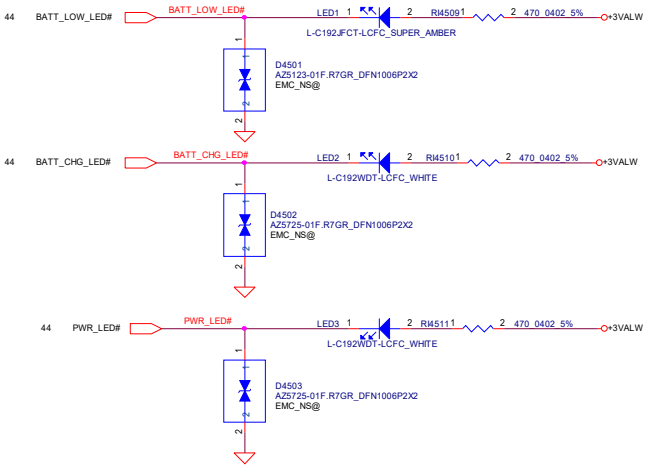
## K/B Connector

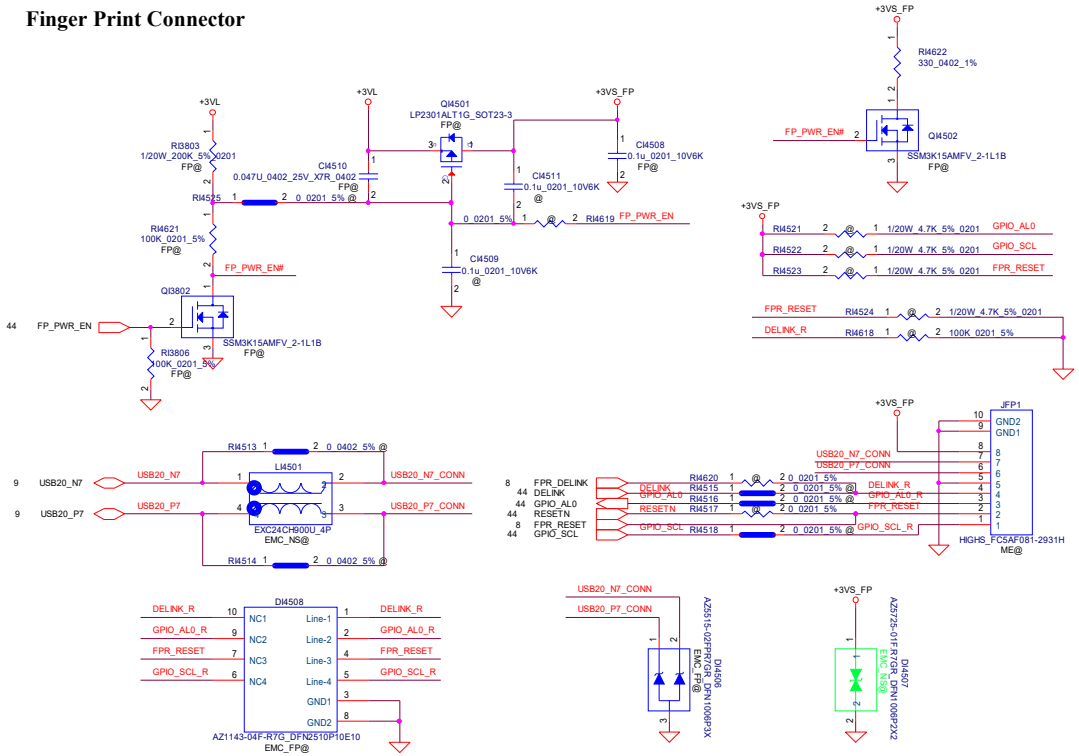



## TP/B Connector

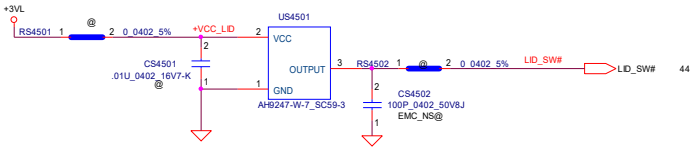



## Finger Print Connector




## HALL Sensor

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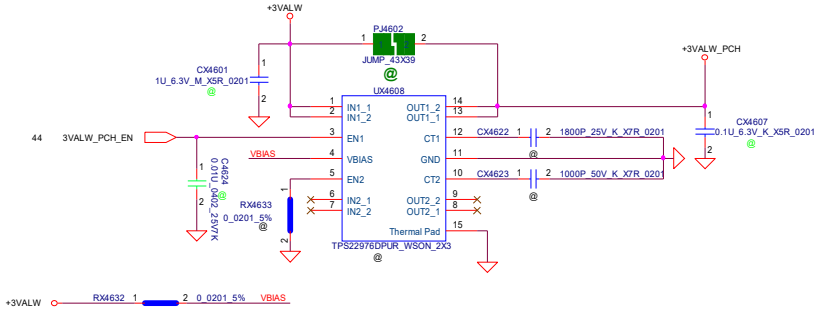
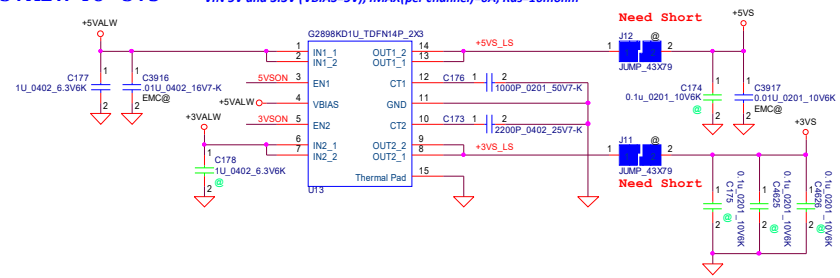
## +3VALW to PCH



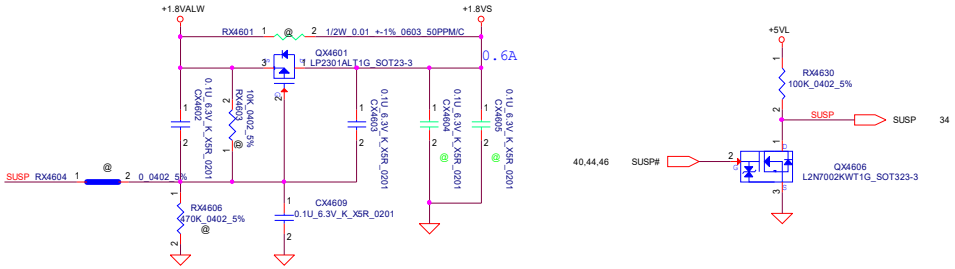

## Load Switch
## +5VALW To +5VS
## +3VALW To +3VS

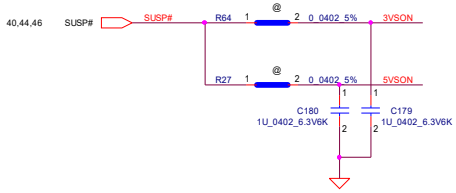
**+3VS, C173 --> 2.74ms**
**+5VS, C176 --> 2.03ms**

*VIN 5V and 3.3V (VBIAS=5V), IMAX(per channel)=6A, Rds=16mohm*

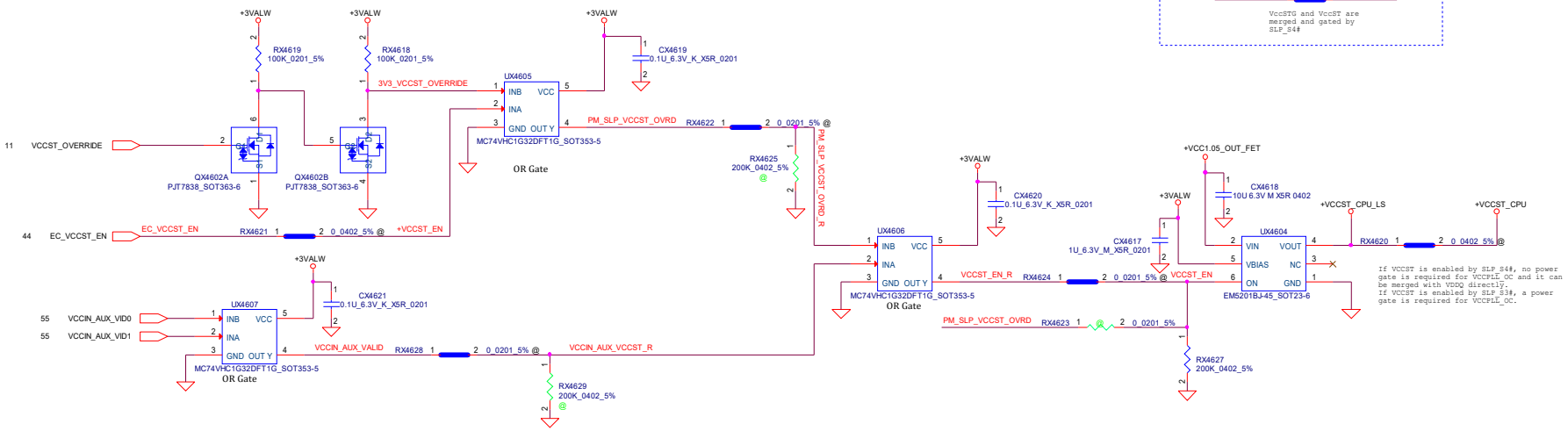



## +1.8VALW to +1.8VS




## VCCST&VCCSTG

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Title: **DC V TO VS INTERFACE**

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|---|---|---|
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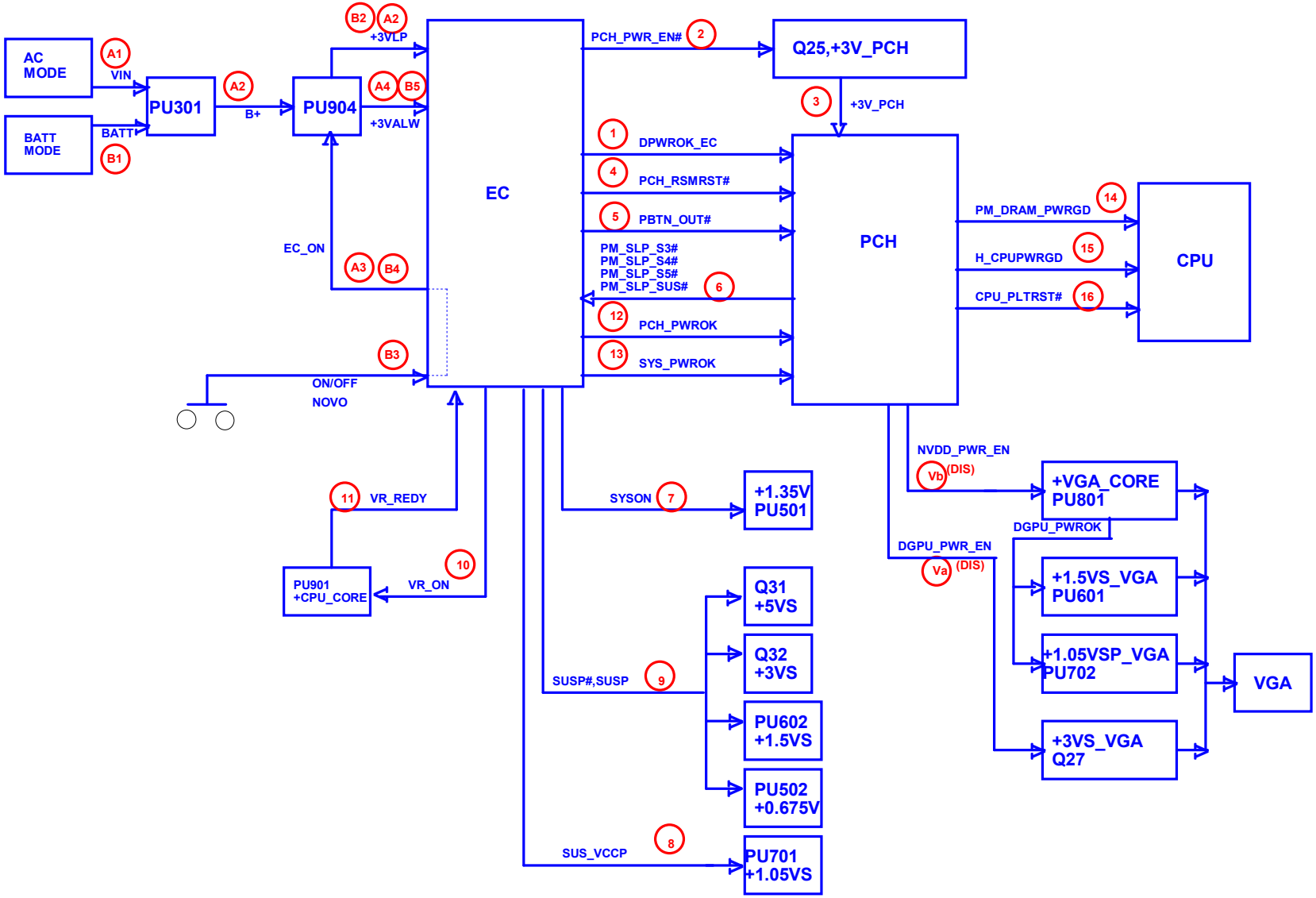


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Title: **Power sequence block**

LCFC

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|---|---|---|
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## CPU

UC1 1035G4@ — MP PN — Intel i5-1035G4 1.1G/4C — SA0000A4T20

UC1 1035G1@ — MP PN — Intel i5-1035G1 1G/4C/6M — SA0000A8W30

UC1 1005G1@ — MP PN — Intel i3-1005G1 1.2G/2C/4M — SA0000A9V10

UC1 1065G7@ — MP PN — Intel i7-1065G7 1.3G/4C/8M — SA0000A4U10

## DRAM_Samsung

ZZZ1 SAM_DRAM@ — D4G SAM — X7648112001

## DRAM_Hynix

ZZZ1 Hyn_DRAM@ — HYNIX D4G — X7648112002

## DRAM_Micron

ZZZ1 Mic_DRAM@ — D4G MIC — X7648112003

## SO_DIMM only

## PCB_MB

ZZZ — NM-D031 — DAZ1JZ00100 — 14@

ZZZ — NM-D031 — DAZ1K000100 — 15@

## HDMI Royalty

ZZZ2 HDMI@ — HDMI PN — RC00000040J

## GPU

RV2317 OPTN17@ — 5.11_0805_1% — SD00001NQ00

RV2317 OPTN16@ — 470_0805_5% — SD00247008J

## VRAM

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Title: *Virtual symbol*

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## PCB Fedical Mark PAD

FD4901 FD4902 FD4903 FD4904 FD4905 FD4906

## CPU Thermal Hole

H4902 HOLEA — PAD_CT7P0B6P0D3P2
H4904 HOLEA — PAD_CT7P0B6P0D3P2
H4906 HOLEA — PAD_CT7P0B6P0D3P2
H4907 HOLEA — PAD_CT7P0B6P0D3P2

## GPU Thermal Hole

H4903 HOLEA — PAD_CT7P0B6P0D3P2
H4905 HOLEA — PAD_CT7P0B6P0D3P2

H4908 HOLEA — PAD_C7P0D4P0
H4909 HOLEA — PAD_C7P0D4P0
H4910 HOLEA — PAD_O2P5X3P0D2P5X3P0N
H4911 HOLEA — PAD_O2P5X3P0D2P5X3P0N

H4912 HOLEA — PAD_C7P0D2P8
H4913 HOLEA — PAD_C7P0D2P8
H4914 HOLEA — PAD_C7P0D2P8
H4901 HOLEA — PAD_C10P0D8P0

H4915 HOLEA — PAD_C7P0D2P4
H4916 HOLEA — PAD_CT7P0B10P0D4P0
H4917 HOLEA — PAD_CT7P0B10P0D4P0

## MD Shielding

SH4901 — SPRING_FINGER_6.2X1.64
SH4902 — SPRING_FINGER_6.2X1.64
SH4903 — SPRING_FINGER_6.2X1.64
SH4904 — SPRING_FINGER_6.2X1.64
SH4905 — SPRING_FINGER_6.2X1.64
SH4906 — SPRING_FINGER_6.2X1.64

## SODIMM Shielding

SH4907 — SHIELDING_SUL-35A2M_9P2X3P3_1P
SH4908 — SHIELDING_SUL-35A2M_9P2X3P3_1P
SH4909 — SHIELDING_SUL-35A2M_9P2X3P3_1P
SH4910 — SHIELDING_SUL-35A2M_9P2X3P3_1P
SH4911 — SHIELDING_SUL-35A2M_9P2X3P3_1P

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Title: **Hole**

Size: B | Document Number: GS44D/GS54D | Rev: 0.1

Date: Friday, December 06, 2019 | Sheet 49 of 60

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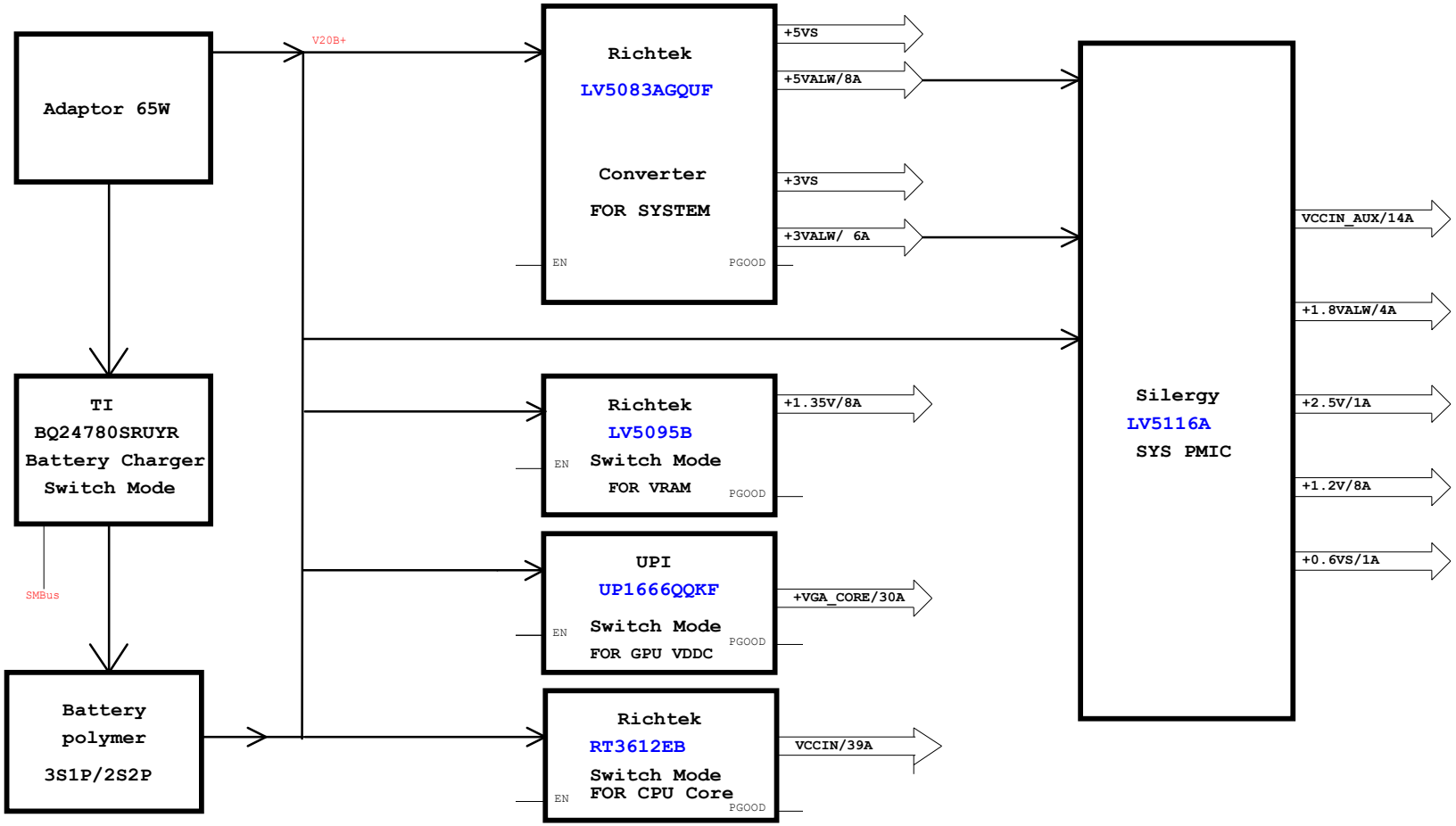


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Title: PWR-Power Diagram

Size: C | Document Number: GS44D/GS54D | Rev: 0.3

Date: Friday, December 06, 2019 | Sheet 50 of 60

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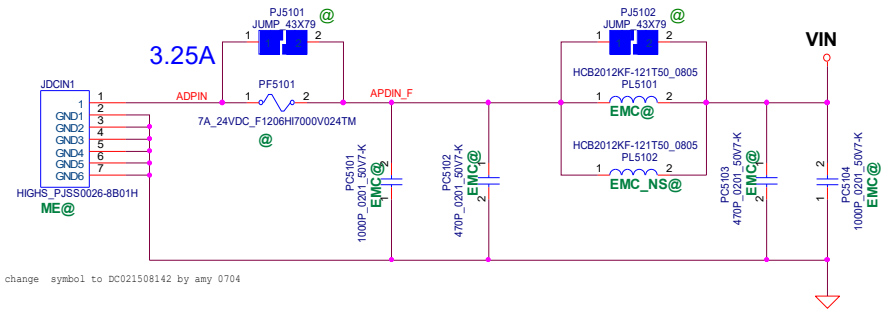
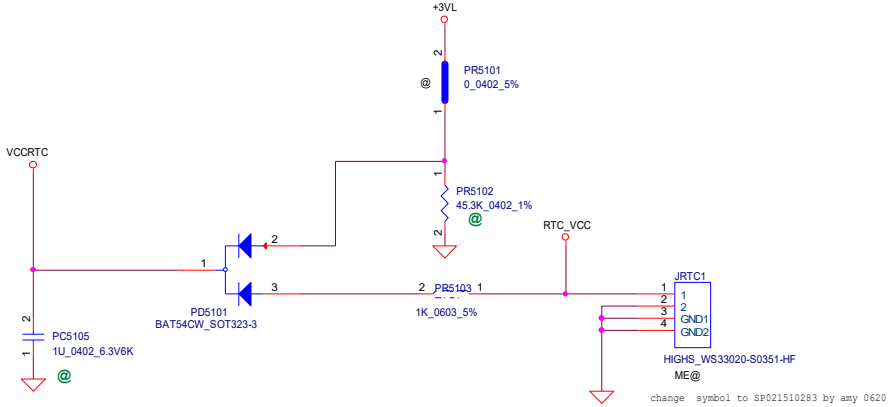



change symbol to DC021508142 by amy 0704




change symbol to SP021510283 by amy 0620

RTC_VCC 20MIL
+3VL 20MIL
VCCRTC 20MIL

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Title: PWR-DCIN / RTC charger

Size: Custom | Document Number: GS44D/GS54D | Rev: 0.3

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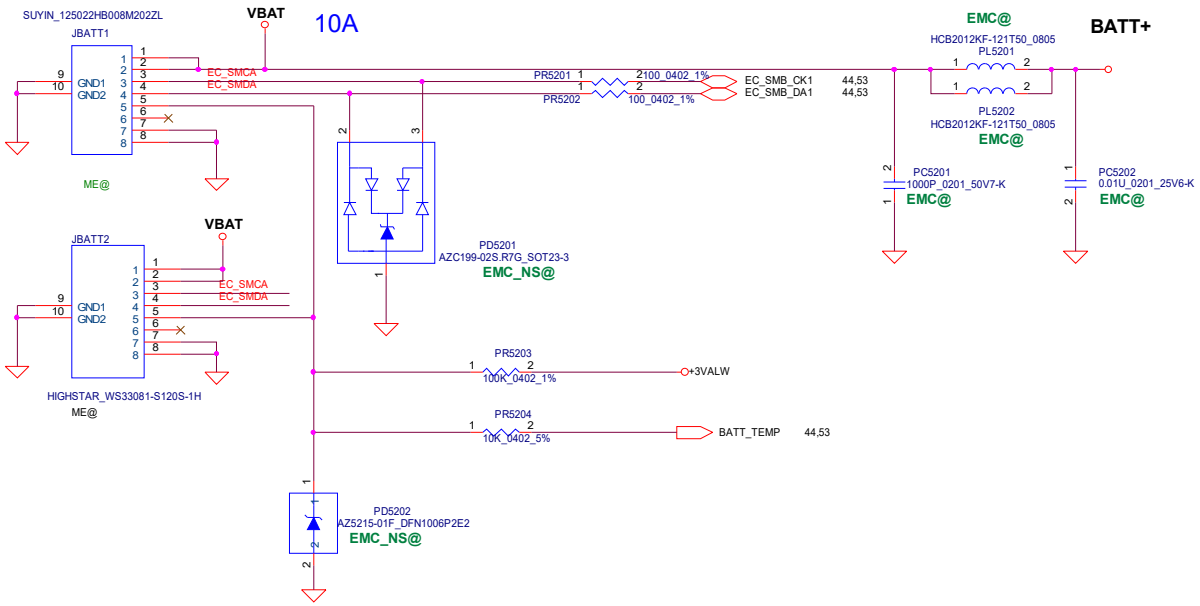


2S1P polymer battery voltage level: +5.5V ~ 8.8 V

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Title: PWR-BATTERY CONN/OTP

Size: Custom | Document Number: GS44D/GS54D | Rev: 0.3

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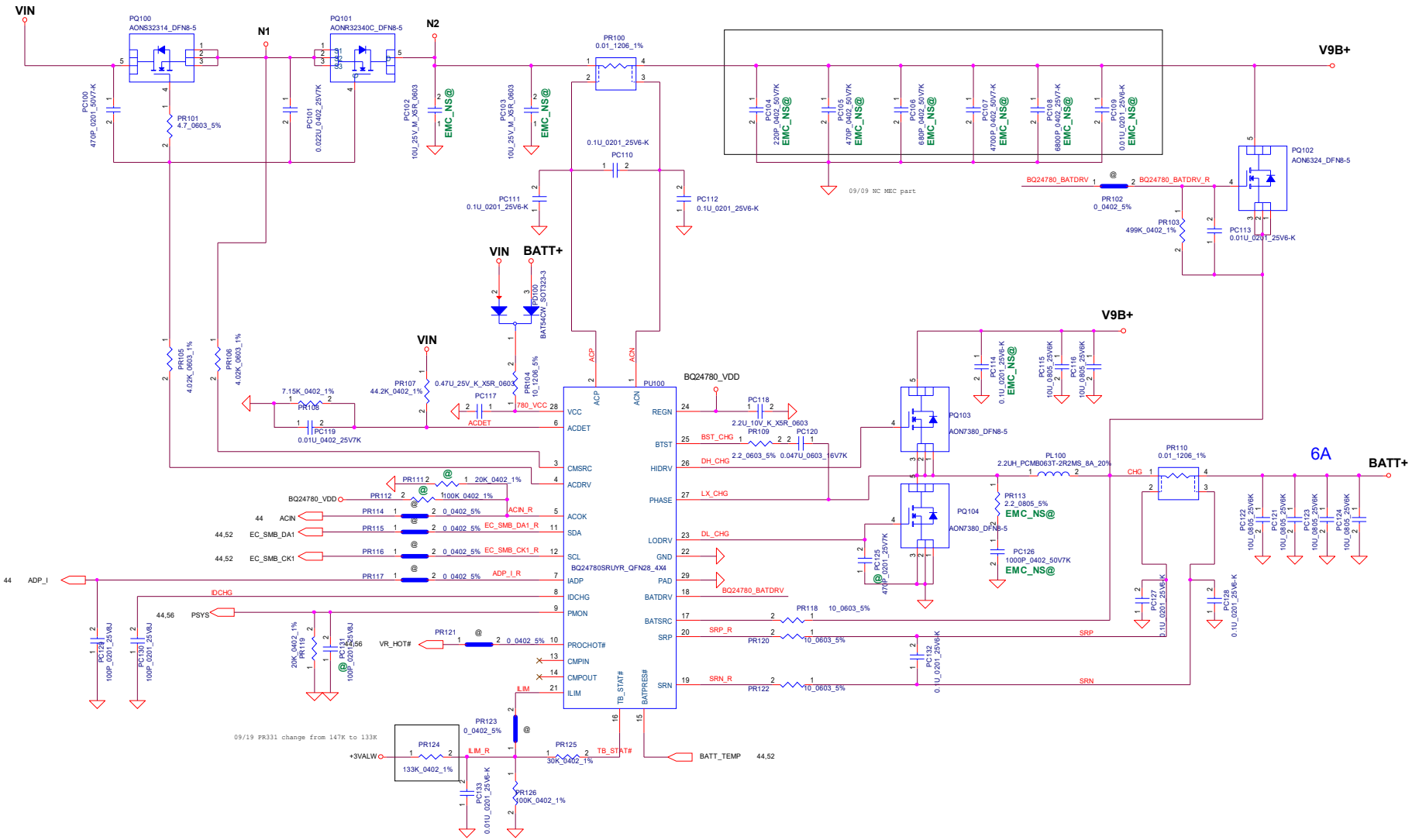


ACDECT setting 17.2V
Charge current limit HW=7A
DC discharge limit =26A
Discharge current limit HW=9A during Turbo boost

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| Issued Date | 2018/07/10 | Deciphered Date | 2018/07/10 |

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Title: PWR-CHARGER

Size: C | Document Number: GS44D/GS54D | Rev: 0.3

Date: Friday, December 06, 2019 | Sheet 53 of 1

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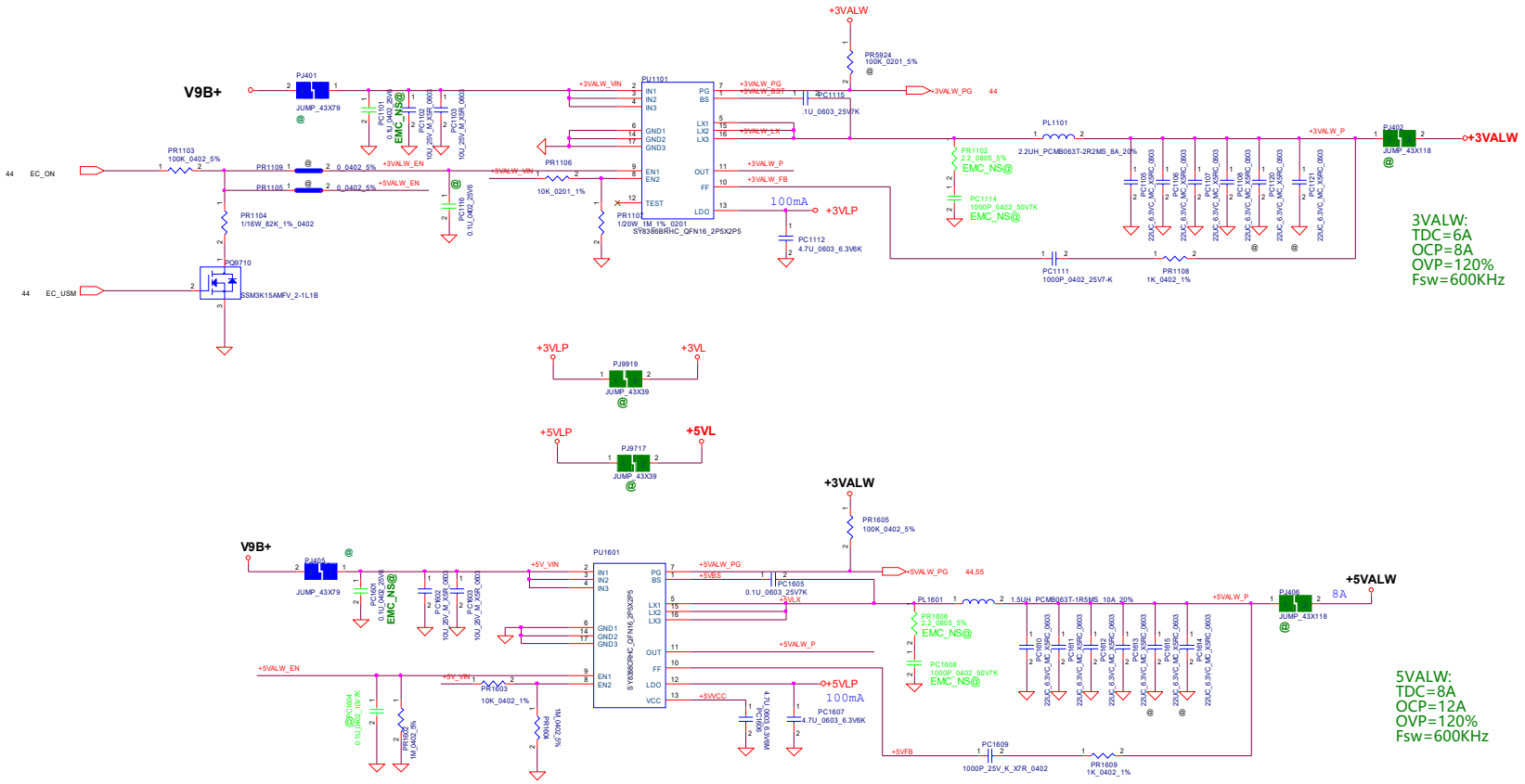


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Title: PWR_3VALW/5VALW

Size: Custom | Document Number: S350 ADA | Rev: 0.3

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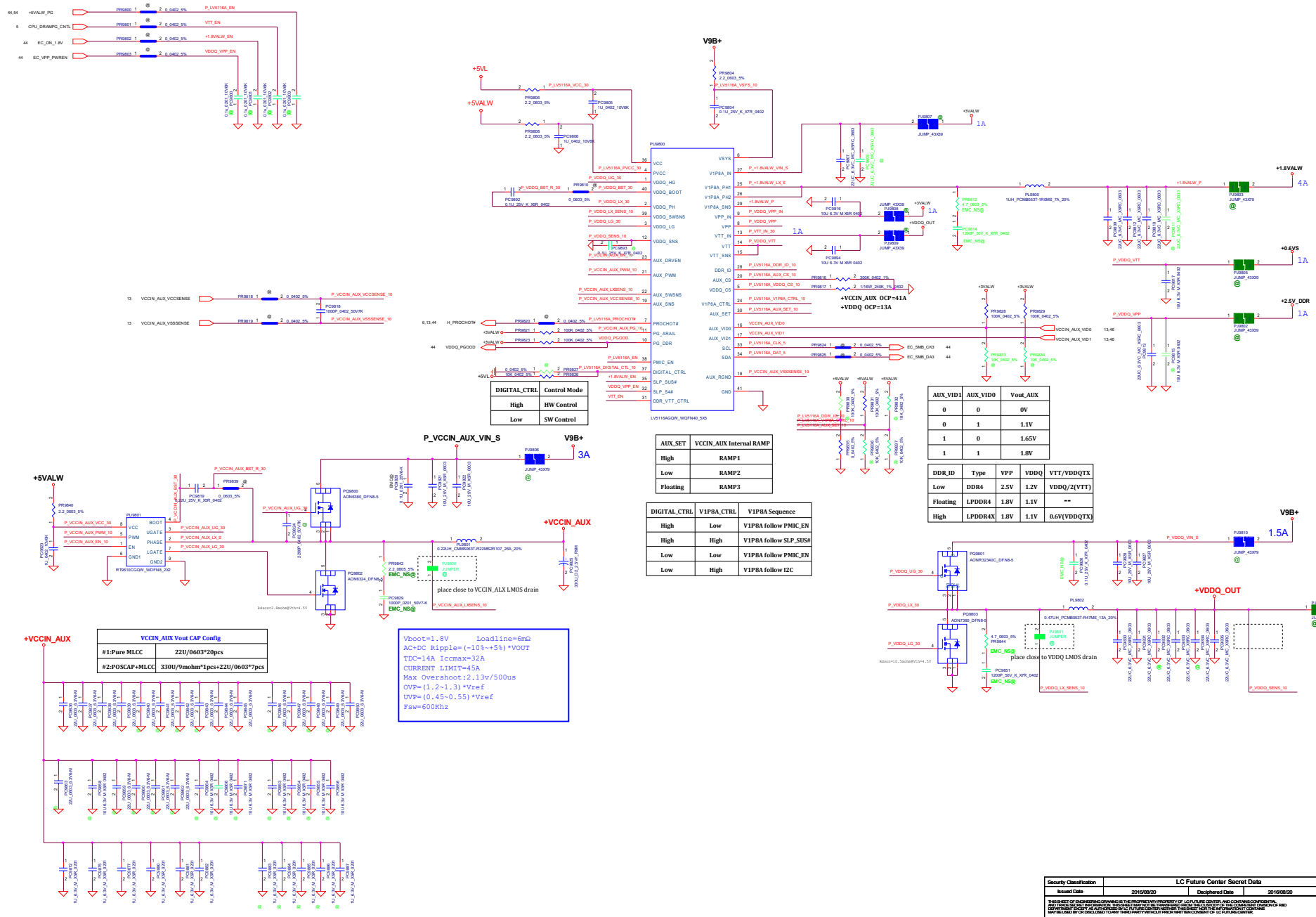


| DIGITAL_CTRL | Control Mode |
|---|---|
| High | HW Control |
| Low | SW Control |

| AUX_SET | VCCIN_AUX Internal RAMP |
|---|---|
| High | RAMP1 |
| Low | RAMP2 |
| Floating | RAMP3 |

| DIGITAL_CTRL | V1P8A_CTRL | V1P8A Sequence |
|---|---|---|
| High | Low | V1P8A follow PMIC_EN |
| High | High | V1P8A follow SLP_SUS# |
| Low | Low | V1P8A follow PMIC_EN |
| Low | High | V1P8A follow I2C |

| AUX_VID1 | AUX_VID0 | Vout_AUX |
|---|---|---|
| 0 | 0 | 0V |
| 0 | 1 | 1.1V |
| 1 | 0 | 1.65V |
| 1 | 1 | 1.8V |

| DDR_ID | Type | VPP | VDDQ | VTT/VDDQTX |
|---|---|---|---|---|
| Low | DDR4 | 2.5V | 1.2V | VDDQ/2(VTT) |
| Floating | LPDDR4 | 1.8V | 1.1V | -- |
| High | LPDDR4X | 1.8V | 1.1V | 0.6V(VDDQTX) |

| VCCIN_AUX Vout CAP Config | |
|---|---|
| #1:Pure MLCC | 22U/0603*20pcs |
| #2:POSCAP+MLCC | 330U/9mohm*1pcs+22U/0603*7pcs |

Vboot=1.8V Loadline=6mΩ
AC+DC Ripple=(-10%~+5%)*VOUT
TDC=14A Iccmax=32A
CURRENT LIMIT=45A
Max Overshoot:2.13v/500us
OVP=(1.2~1.3)*Vref
UVP=(0.45~0.55)*Vref
Fsw=600Khz

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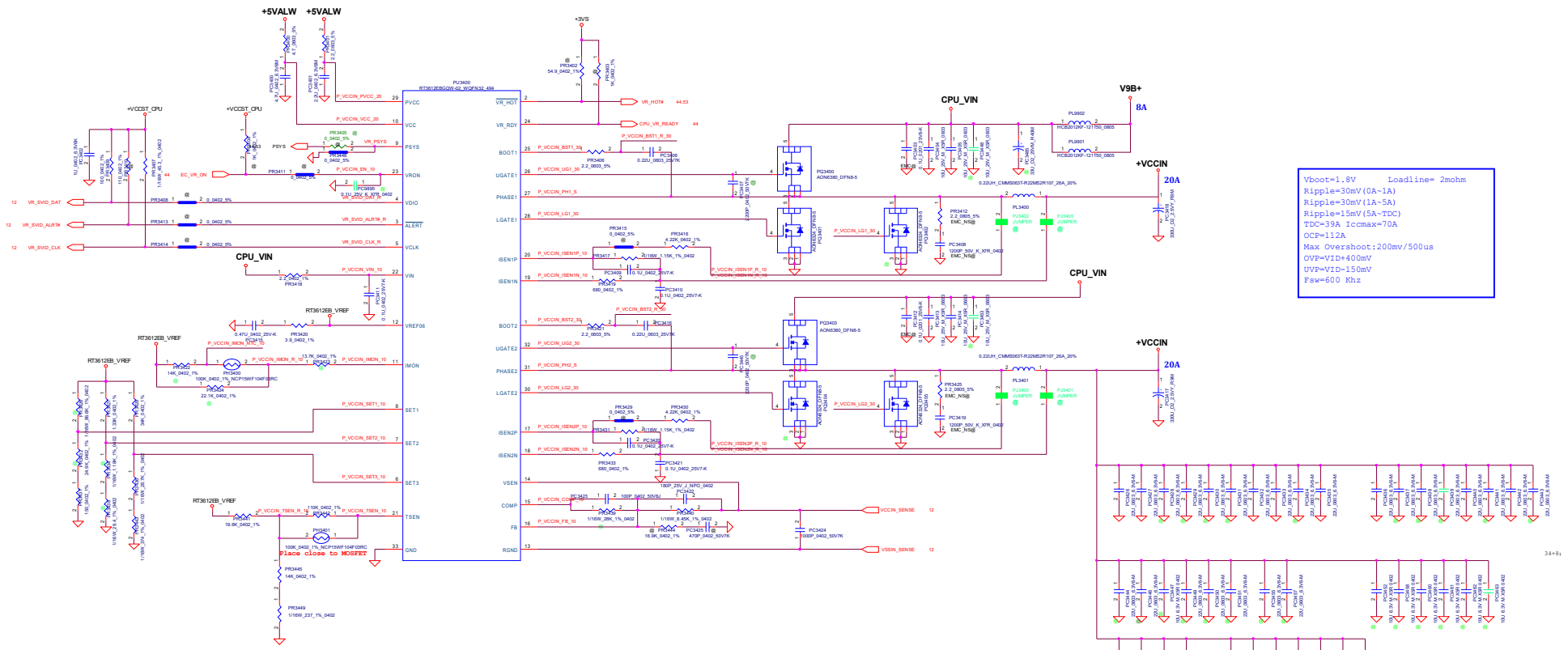


Vboot=1.8V Loadline= 2mohm
Ripple=30mV(0A~1A)
Ripple=30mV(1A~5A)
Ripple=15mV(5A~TDC)
TDC=39A Iccmax=70A
OCP=112A
Max Overshoot:200mv/500us
OVP=VID+400mV
UVP=VID-150mV
Fsw=600 Khz

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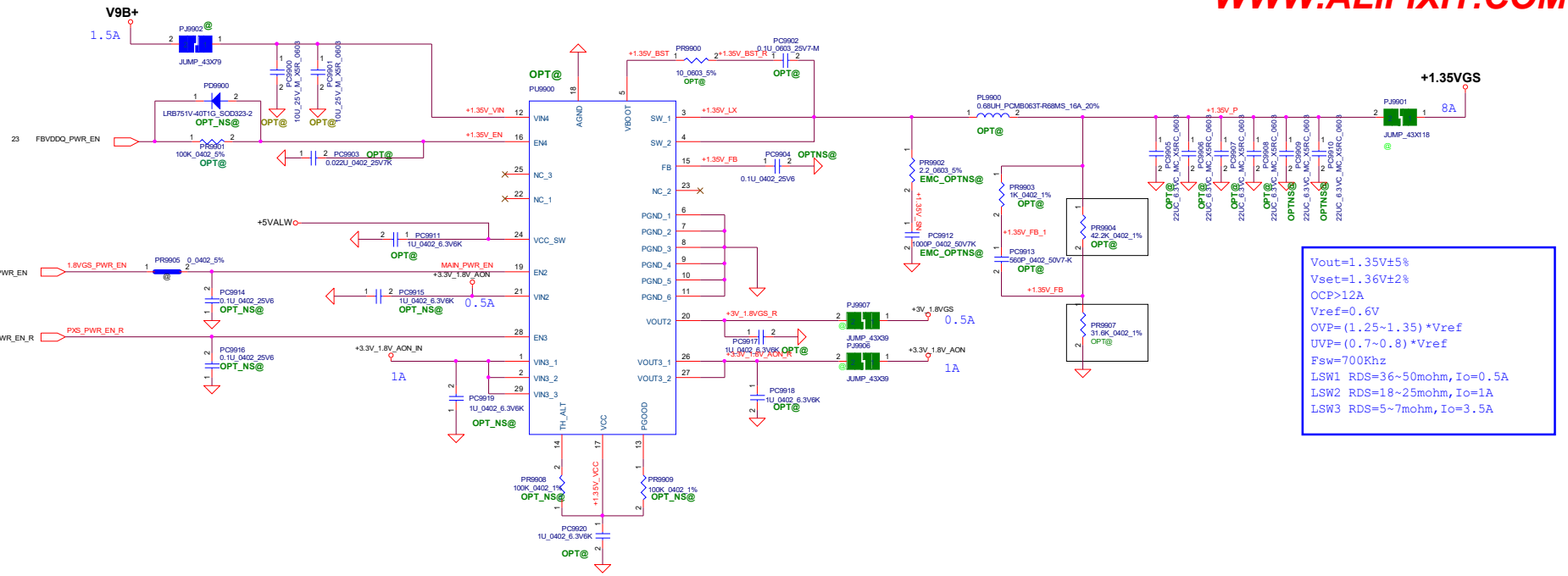
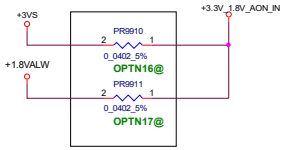
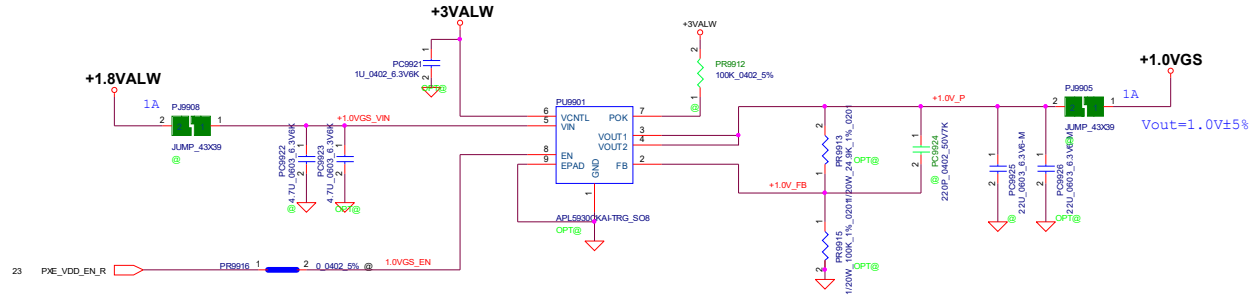



Vout=1.35V±5%
Vset=1.36V±2%
OCP>12A
Vref=0.6V
OVP=(1.25~1.35)*Vref
UVP=(0.7~0.8)*Vref
Fsw=700Khz
LSW1 RDS=36~50mohm,Io=0.5A
LSW2 RDS=18~25mohm,Io=1A
LSW3 RDS=5~7mohm,Io=3.5A

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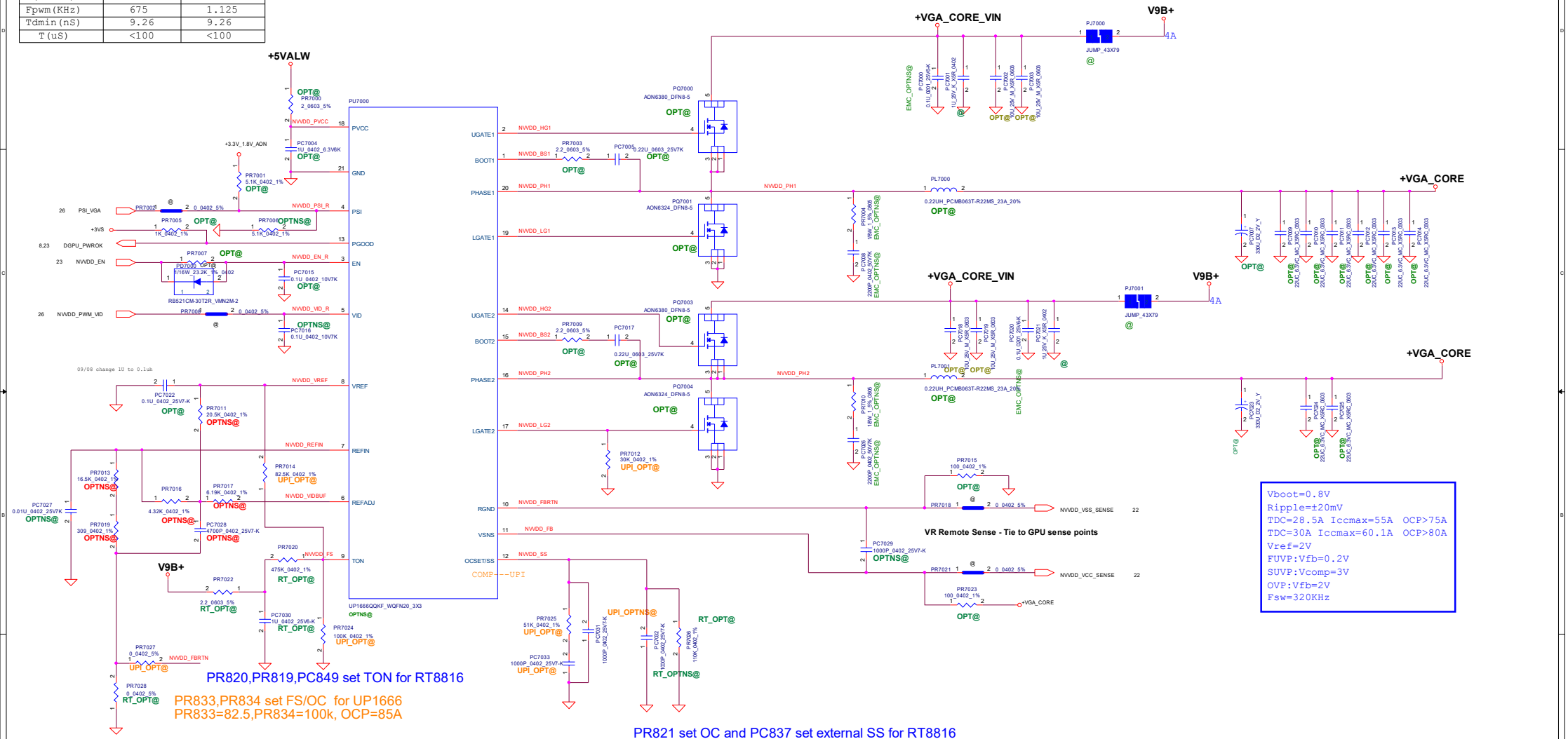
| PWM-VID Specification | | |
|---|---|---|
| | N17 Config | N16 Config B |
| Vmin(V) | 0.3 | 0.6 |
| Vmax(V) | 1.3 | 1.2 |
| Vboot(V) | 0.8 | 0.9 |
| Vstep(mV) | 6.25 | 6.25 |
| N(level) | 160 | 96 |
| Fpwm(KHz) | 675 | 1.125 |
| Tdmin(nS) | 9.26 | 9.26 |
| T(uS) | <100 | <100 |

| RT8816 PSI | UP1666 PSI | Phase Configuration |
|---|---|---|
| 1.6V~5.5V | 1.6~5.5V | 2Phase CCM |
| 1.08~1.35V | 1~1.4V | 2Phase DEM |
| 0.7~0.88V | 0.4V~0.8V | 1Phase CCM |
| 0~0.4V | 0~0.2V | 1Phase DEM |




Vboot=0.8V
Ripple=±20mV
TDC=28.5A Iccmax=55A OCP>75A
TDC=30A Iccmax=60.1A OCP>80A
Vref=2V
FUVP:Vfb=0.2V
SUVP:Vcomp=3V
OVP:Vfb=2V
Fsw=320KHz

PR820,PR819,PC849 set TON for RT8816

PR833,PR834 set FS/OC for UP1666
PR833=82.5,PR834=100k, OCP=85A

PR821 set OC and PC837 set external SS for RT8816
PR832,PC834,PR836 set COMP for UP1666

PR816,PR812,PR815,PR813,PR818,PC826 BOM structure control for N16 or N17

| Component | Value | N17 | N16 |
|---|---|---|---|
| R1(KΩ) | PR7017 | 6.19 | 20 |
| R2(KΩ) | PR7011 | 20.5 | 20 |
| R3(KΩ) | PR7016 | 4.32 | 2 |
| R4(KΩ) | PR7013 | 16.5 | 18 |
| R5(KΩ) | PR7019 | 0.309 | 0 |
| C(nF) | PC7028 | 4.7 | 2.7 |

UPI_OPT@ : for UP1666
RT_OPT@ : for RT8816A

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| | | | | | | | |
|---|---|---|---|---|---|---|---|
| U42@ | U42@ | U42@ | U42@ | U42@ | U42@ | U42@ | U42@ |
| PR3423 | PR3424 | PR3422 | PR3439 | PR3426 | PR3432 | PR3434 | PR3438 |
| 13.7K +-1% 0402 | 22.1K +-1% 0402 | 14K +-1% 0402 | 28K +-1% 0402 | 86.6K +-1% 0402 | 24.9K +-1% 0402 | 1.18K +-1% 0402 | 29.4 +-1% 0402 |
| SD03413728J | SD03422128J | SD03414028J | SD000015J00 | SD00001PM00 | SD03424928J | SD00001DI00 | SD00001BC00 |
| U22@ | U22@ | U22@ | U22@ | U22@ | U22@ | U22@ | U22@ |
| PR3423 | PR3424 | PR3422 | PR3439 | PR3426 | PR3432 | PR3434 | PR3438 |
| 20.5K +-1% 0402 | 25.5K +-1% 0402 | 11.5K +-1% | 24.3K +-1% | 130K +-1% 0402 | 22.6K +-1% 0402 | 1.1K +-1% 0402 | 40.2 +-1% 0402 |
| SD03420528J | SD03425528J | SD03411528J | SD000011300 | SD03413038J | SD000019W00 | SD03411018J | SD034402A8J |

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